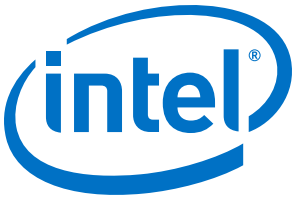

AN 835: PAM4 Signaling Fundamentals

AN-835 | 2019.03.12
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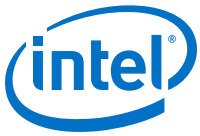


1. Introduction

This Pulse-Amplitude Modulation 4-Level (PAM4) application note explains PAM4 theory and operation while introducing the Intel® Stratix® 10 TX device capability and the realization of 57.8 Gbps data rate applications.

The application note uses 56 Gbps to describe data rates in general because of the baseline established in the Common Electrical Interface (CEI). However, the actual data rate can be up to 57.8 Gbps.

1.1. NRZ Fundamentals

Ethernet is a family of computer networking technologies that is most widely used in local area networks (LAN), metropolitan area networks (MAN) and wide area networks (WAN).

Since its commercial introduction in 1980 and first standardization in 1983, Ethernet continues to support increasing demands for a connected world with instant data transmission. Development of 100G Ethernet is currently underway. Achieving greater Ethernet speeds like 200G/400G requires a significant technological advancement. Two coding schemes are possible: Non-Return-to-Zero (NRZ), also known as Pulse-Amplitude Modulation 2-Level (PAM2), and Pulse-Amplitude Modulation 4-Level (PAM4). Because of NRZ's higher Nyquist frequency which results in higher channel-dependent loss, PAM4 has become a more viable solution.

NRZ is a modulation technique that has two voltage levels to represent logic 0 and logic 1. PAM4 uses four voltage levels to represent four combinations of two bits logic – 11, 10, 01, and 00. Refer to *Standards Using PAM4 Coding Scheme* for more details about PAM4 naming conventions. Each of the modulation schemes comes with a unique set of advantages and disadvantages.

Figure 1. NRZ (PAM2) and PAM4 Coding

Compared with NRZ, PAM4 has the advantages of having half the Nyquist frequency and twice the throughput for the same Baud rate (28 GBaud PAM4 = 56 Gbs) since each voltage level ("symbol") represents two bits of information. The PAM4 case is not gray encoded.

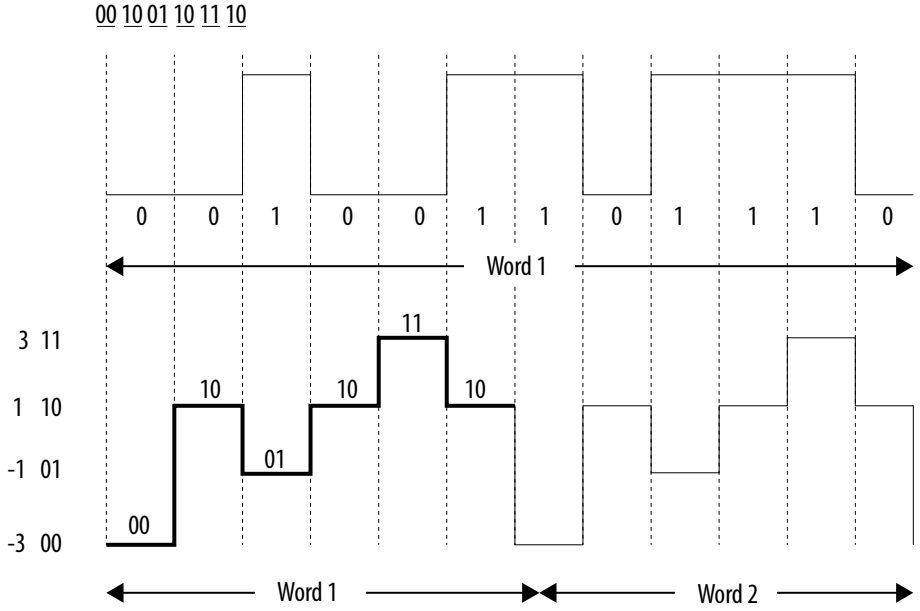
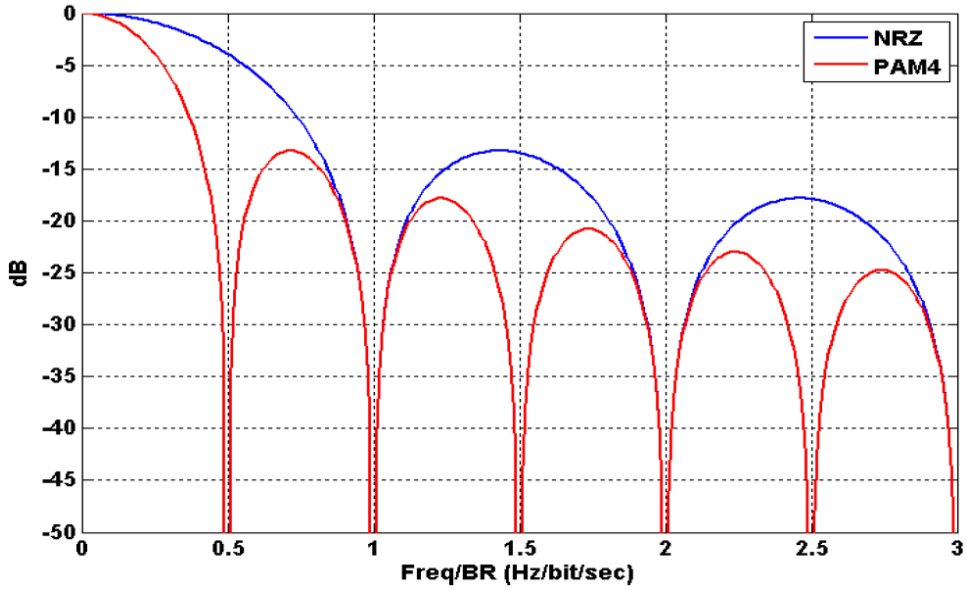


Figure 2. Power Spectrum Density of NRZ and PAM4

At 56 Gbps, PAM4 requires half of the Nyquist frequency as that of NRZ.



PAM4 $f_{Nyquist}$ = 56/4 = 14 GHz (Figure 1 on page 5)

NRZ $f_{Nyquist}$ = 56/2 = 28 GHz (Figure 2 on page 5)

Many benefits are associated with having half the Nyquist frequency. These include: doubling the density of data, achieving higher resolution using the same oversampling rate, and having the same total noise power spread over a wider frequency so that the noise power in bandwidth goes down. However, there are some disadvantages. The PAM4 signal has 1/3 the amplitude of that of a similar NRZ signal. Therefore, the PAM4 signal has a worse Signal-to-Noise Ratio (SNR). Because of the tighter spacing between voltage levels in PAM4 signaling, a PAM4 signal is more susceptible to noise. When all non- linearity effects are added, the SNR loss is approximately 11 dB.

Equation 1. SNR Loss

The SNR loss of a PAM4 signal compared to an NRZ signal is ~9.5 dB

$$\text{SNR loss} = 20 \times \log_{10}\frac{1}{3} \approx -9.5\,\text{dB}$$

A transceiver implementing PAM4 is expected to be more complex and consume higher power than a transceiver supporting NRZ because of the need for more advanced equalization. Because of this complexity, you must determine when using PAM4 is more advantageous than NRZ.

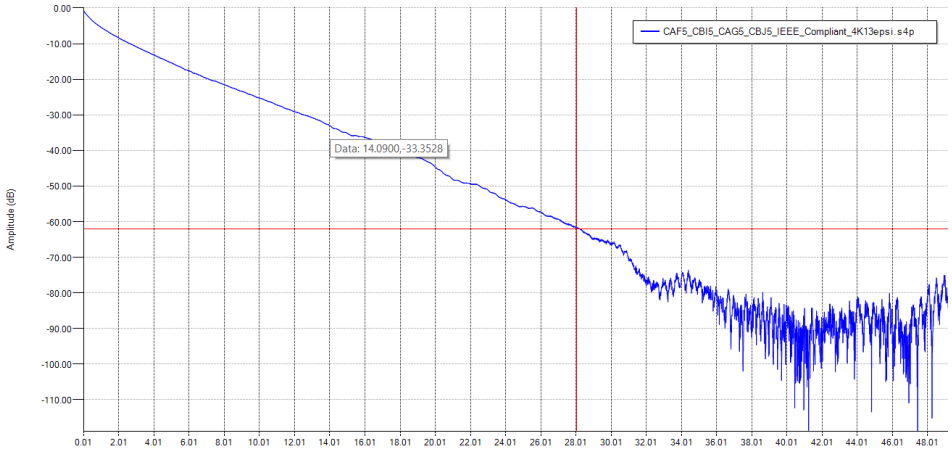
The insertion loss for a Nyquist frequency of 14 GHz on a sample IEEE 802.3 compliant backplane is approximately 33.35 dB.

The same backplane shows an insertion loss of approximately 62 dB for a Nyquist of 28 GHz.

These insertion loss numbers clearly show that it would be much more challenging to equalize the backplane using NRZ than it would when using PAM4.

As shown in the equation for SNR loss, there is a penalty to SNR by using PAM4. However, that penalty is considerably lower than the approximately 11 additional dB that would need to be equalized for the same backplane. Designers can try to minimize insertion loss by using better materials. However, that approach is not possible for legacy systems which are already deployed in the field.

Figure 3. Channel Insertion Loss vs. Nyquist Frequency



Intel Stratix 10 family incorporates next-generation transceiver technology to realize today's large-scale data centers, cloud computing, and wireless applications that require increased bandwidth at lower power and minimum cost per bit. The dual-mode transceivers that are capable of 57.8 Gbps PAM4 and 28.9 Gbps NRZ enable the next-

generation high speed interconnects while minimizing insertion loss and crosstalk at terabit data rates. The new standard supports both optical and copper interfaces for chip-to-chip, backplane and direct attach cable applications.

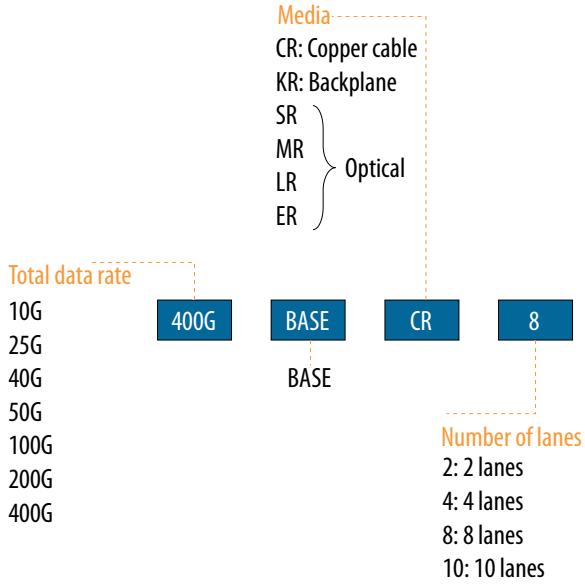
Related Information

Standards Using PAM4 Coding Scheme on page 7

1.2. Standards Using PAM4 Coding Scheme

Protocol names typically include information about protocol characteristics such as data rate and transmission media. For example, 400GBASE-CR8 is an 8-lane protocol that can achieve a 400 Gbps data rate (with each lane running at 53.125 Gbps). The CR8 part of the name means that signals are traveling through 8 lanes of copper cable.

Figure 4. Sample of a Protocol Name and Available Options



In many electrical interface standards such as the Attachment Unit Interface (AUI), the data rate can be derived from the roman numerals in the protocol names:

Table 1. Roman Numerals

Symbol	I	V	X	L	C	D	M
Value	1	5	10	50	100	500	1000

By decoding the roman numerals in the protocol names, XAUI has a 10 Gbps data rate, CAUI has a 100 Gbps data rate and CDAUI has a 400 Gbps data rate .

Note: If a smaller number appears before a larger number, it is subtracted from the larger number. For example, CDAUI has a data rate of D-C=500-100=400 Gbps. Conversely, if a larger number appears before a smaller number, it is added to the smaller number.

Many standards (such as 400GBASE-SR16) use the PAM4 coding scheme. This 400-Gbps interface uses the Short Reach 100-meter distance optical media protocol. It uses the QSFP-DD pluggable module. The electrical interface is 400GUI-16 or 400GUI-8, which means each lane operates at 26.5625 Gbps or 53.125 Gbps.

200GBASE-KR4 is a standard for a 200 Gbps backplane with four lanes running at a 53.125 Gbps lane rate. It reaches a distance of 0.5 to 1 meter.

100GBASE-CR2 is a 100 Gbps, 3-meter distance protocol using copper cables as media with a 53.125 Gbps lane rate. 100GBASE-CR2 is used in the rack between the server and the top-of-rack Ethernet switch, or between the appliance, router, switch, and server. It uses QSFP56, QSFPDD as the pluggable module.

The exact data rate for the PAM4 signal is determined as follows:

Equation 2. Data Rate per Lane

$$\text{PCS encoding ratio} = \frac{257}{256}$$

$$\text{RS FEC}(544, 514)\ \text{ratio} = \frac{544}{514}$$

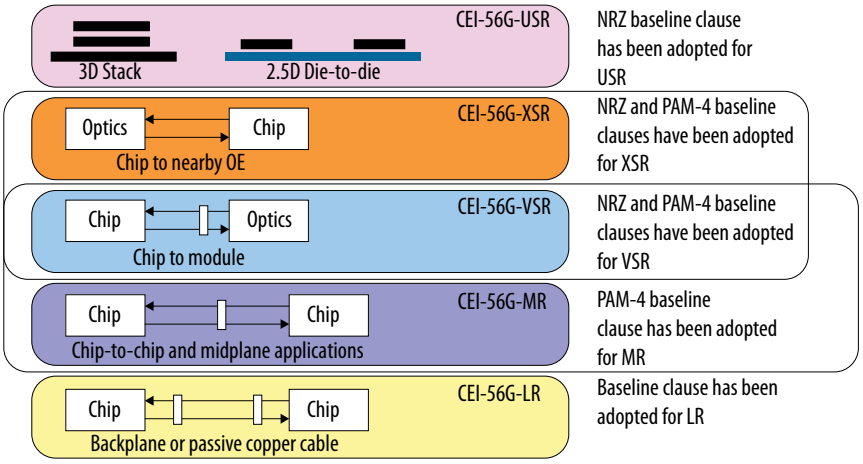
$$\frac{544}{514} \times \frac{257}{256} \times 50 = 53.125\ \text{Gbps}$$

1.3. CEI-56G Interconnect Reaches and Application Distances

Optical Internetworking Forum (OIF) is a non-profit consortium that promotes the development and deployment of interoperable computer networking products and services through implementation agreements (IAs) for optical networking products and component technologies including devices with transceivers.

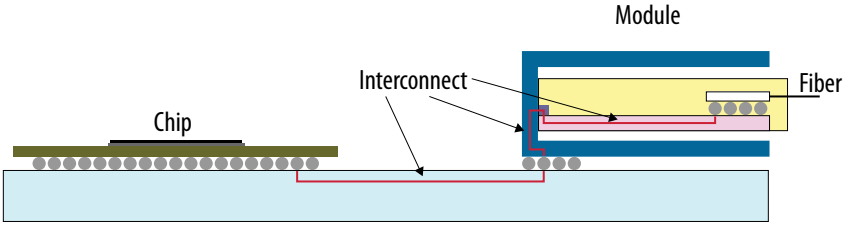
Figure 5. Interconnect Reaches and Application Distances

Summary of the baseline roadmap for CEI-56G serial links.



1.3.1. VSR (Very Short Reach) Chip-to-Module

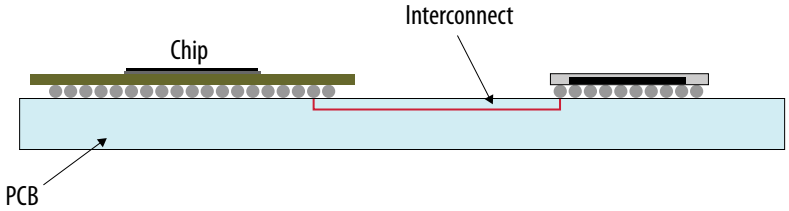
Figure 6. VSR Interconnect



Most modern communication systems support pluggable modules at the front faceplate of the equipment. The electrical link that connects these pluggable modules can extend up to 10 cm. Advanced modulation formats (such as PAM or Discrete Multitone (DMT) schemes), Forward Error Correction (FEC) and equalization features are all possible solutions for the chip-to-module interconnect. This interface can include a single connector.

1.3.2. MR (Mid-Range Reach) - Chip to Chip Within a PCBA

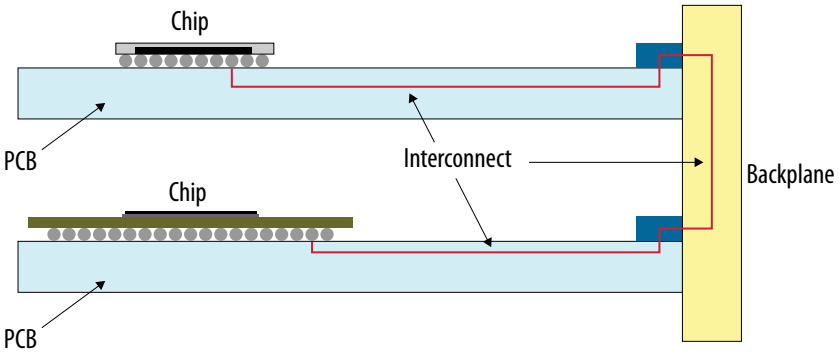
Figure 7. MR Interconnect



An interconnect interface may be needed between two chips on the same Printed Circuit Board Assembly (PCBA) or on a daughter card or shorter mid-plane. By definition, this interface is relatively short ranging up to 50 cm. This interface may include a single connector.

1.3.3. LR (Long Reach) - Chip to Chip Across a Backplane/Midplane or a Cable

Figure 8. LR Interconnect



This interface communicates between two cards across a backplane or midplane within a chassis and is less than 1 meter with up to two connectors. KP-FEC may be a requirement to meet the BER.

Table 2. Summary of CEI 56G Different Reaches and Distances

Parameter	Ultra Short Reach (USR)	Extra Short Reach (XSR)	VSR	MR	LR
Reach	2.5D/3D	Chip- to-optics Engine	Chip- to-module	Chip-to-chip	Chip-to-chip over a backplane
Data Rate (Gbps)	19.6-58	39.2-58	39.2-58	36-58	36-58
BER (pre-FEC)	1E-15	1E-15	1E-6	1E-6	1E-4
Distance	10 mm (~0.4")	50 mm (~2")	150 mm (~6")	500 mm (~20")	1000 mm (~40")
Interconnect	MCM	PCB+0 connector	PCB+1 connector	PCB+1 connector	PCB+2 connectors
Insertion Loss (dB)	2@28 GHz (NRZ)	4@14 GHz (PAM4)	10@14 GHz (PAM4)	20@14 GHz (PAM4)	30@14 GHz (PAM4)
Modulation	NRZ	PAM4 or NRZ	PAM4 or NRZ	PAM4 or NRZ	PAM4 or ENRZ
FEC	No	No	Yes/No	Yes/No	Yes/No

Table 3. Summary of Ethernet 50G/Lane Standards

Reach	400GBE (802.3bs)	200GBE (802.3bs, .cd)	100GBE (802.3cd)	50GBE (802.3cd)
Chip-to-chip (C2C) and Chip-to-module (C2M)	400GAUI-8	200GAUI-4	—	—
Backplane (BP)	—	200GBASE-KR4	100GBASE-KR2	50GBASE-KR
Copper Cable (CC)	—	200GBASE-CR4	100GBASE-CR2	50GBASE-CR

2. CEI-56G-MR Transmitter

This section discusses the CEI-56G-MR transmitter electrical specifications, jitter methodologies and terms and the pre-emphasis method.

2.1. Naming Conventions

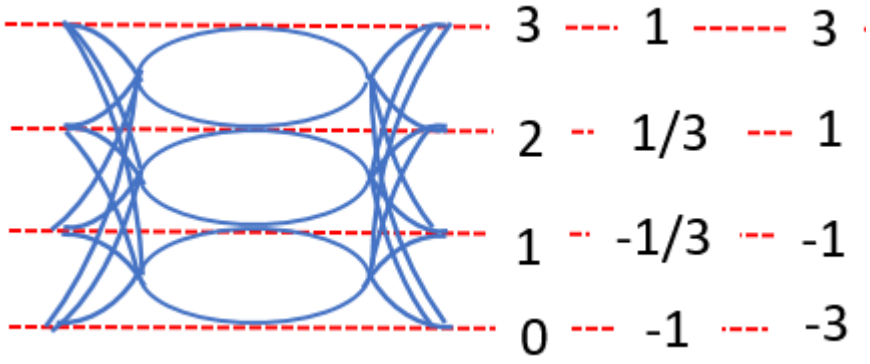
PAM4 uses four voltage levels to represent four combinations of 2 bits logic: 11, 10, 01, and 00. Every two bits are mapped to one symbol. The mapping method can be linear coding or gray coding (see the following table for more details). All PAM4 standards support gray coding.

Table 4. Linear and Gray Coding

Linear Coding	Gray Coding
11	10
10	11
01	01
00	00

Instead of one eye in the NRZ coding scheme, there are three eyes in PAM4 because of the four voltage levels. The naming conventions represent these four voltage levels: -3, -1, 1, 3 or -1, -1/3, 1/3, 1 or 0, 1, 2, 3.

Figure 9. Three PAM4 Signal Levels Naming Conventions

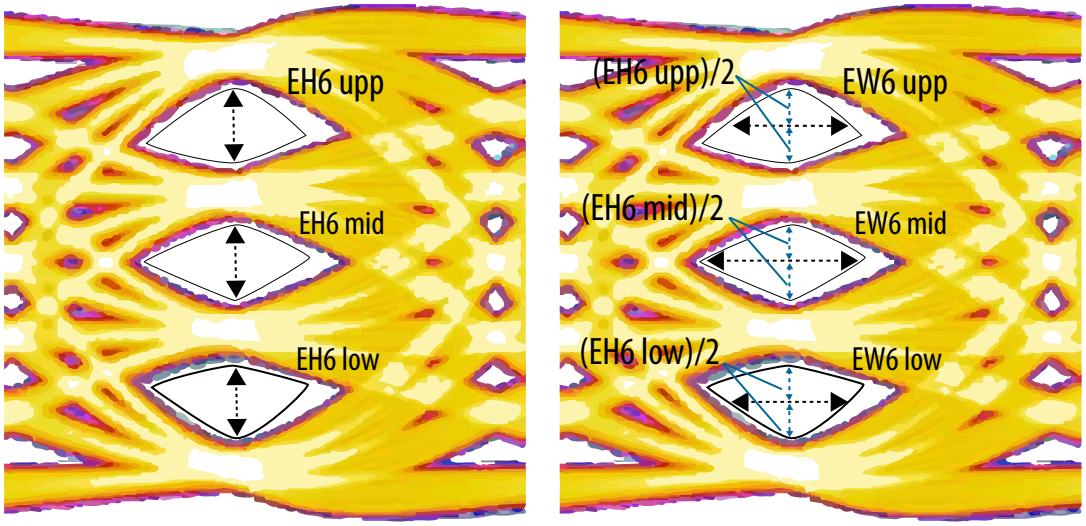


2.2. Eye Height (EH6) and Eye Width (EW6)

When using NRZ, the eye height and width are measured from the biggest opening of an eye. However, this is not the case for PAM4's eye height and eye width.

For the PAM4 eye, one needs to locate the T_{mid} point first. See the following figure for more details. T_{mid} is the midpoint of the maximum horizontal eye opening for a 10^{-3} (this methodology is defined in section 16.3.10.2 of the OIF-CEI56G-VSR standard) inner eye contour (red) of the middle eye.

Figure 10. How EW6 and EH6 Are Measured

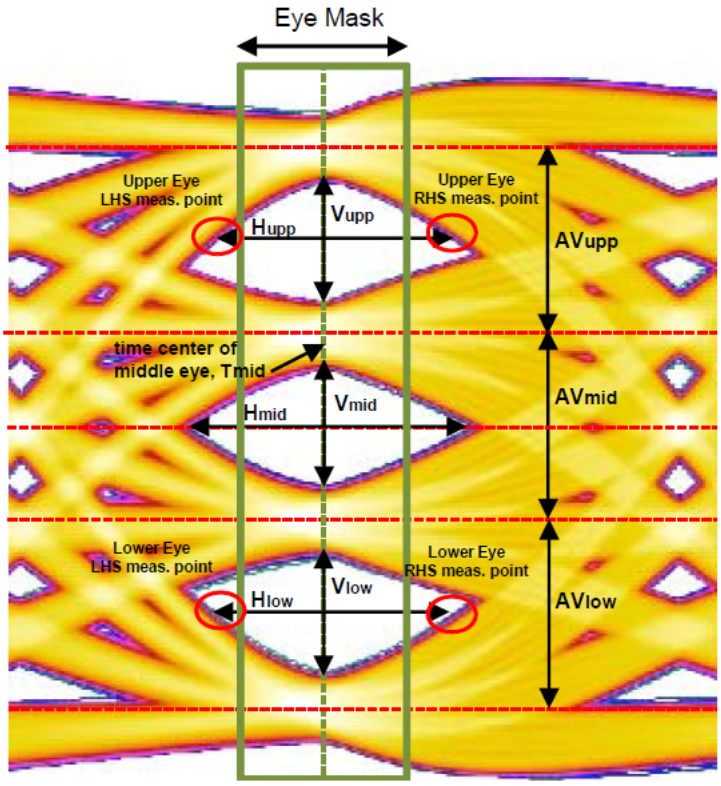


EH6 represents the eye height at a BER of 10^{-6} (green). After the T_{mid} point is found, draw a vertical line that intersects with the three eyes' 10^{-6} contour ring (green). EH6 is the vertical distance between two intersection points on the 10^{-6} contour ring in an eye. As shown in the previous figure, EH6 is not necessarily the maximum eye height.

EW6 represents the eye width at a BER of 10^{-6} (green). Taking the upper eye for example, you find the half point of the eye height, (EH6 upp)/2. Draw a horizontal line that intersects with the 10^{-6} contour ring (green). The EW6 of the upper eye is the horizontal distance between two intersection points on the 10^{-6} contour ring in the eye. The lower eye's EW6 is measured in the same manner. From the figure, notice that the EW6 of each eye is not the widest opening. The asymmetry of the upper and lower eye causes the widest portion of the eye to be off-center. Compared with the widest portion, EW6 is considerably reduced.

This methodology can be used to determine the expected eye mask for a signal for a given BER as per the following figure.

Figure 11. PAM4 Horizontal Eye Mask Sample



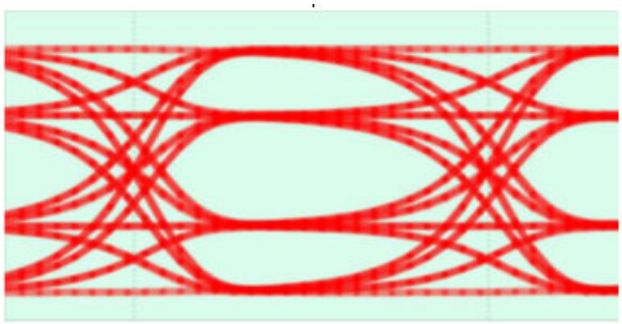
2.3. Eye Linearity

Because deterministic jitter is predictable when compared to random jitter, you can design your transmitter and receiver to eliminate it. Pre-emphasis is used by the transmitter to mitigate deterministic jitter. With good eye linearity, noise will be linear and can be modeled as a linear function. Eye linearity is an alternative to the R_{LM} measurement and is defined in the following equation. Refer to the *Transmitter Linearity (R_{LM})* section for more details. The AVupp, AVmid and AVlow are the averages of the eye amplitudes, not EH6, as shown in the following figure. An ideal PAM4 eye has an eye linearity of 1.

Equation 3. Eye Linearity

$$\text{Eye Linearity} = \frac{\min(AV_{upp}, AV_{mid}, AV_{low})}{\max(AV_{upp}, AV_{mid}, AV_{low})}$$

Figure 12. Non-Linear Eye Linearity



Related Information

Transmitter Linearity (RLM) on page 17

2.4. Electrical Characteristics

2.4.1. Transmitter Characteristics

The following table defines the basic transmitter characteristics for an OIF-CEI56G-MR interface.

Table 5. Transmitter Electrical Output Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		18.0		29.0	Gsym/s
Output Differential Voltage	T_Vdiff	See (1), (2)			1200	mVppd
DC Common Mode Voltage	T_Vcm	See (3)	0		1.9	V
Output AC Common Mode Voltage	T_VcmAC	See (4), (5)			30	mVrms

continued...

(1) Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.

(2) Measured as described in Section 17.3.1.2.

(3) Measured as described in Section 17.3.1.2. of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04

(4) Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.

(5) Measured as described in Section 17.3.1.2 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Single-Ended Transmitter Output Voltage	T_Vse	See (6), (7)	-0.3		1.9	V
Differential Output Return Loss	T_SDD22	(8)				dB
Common Mode Output Return Loss	T_SCC22	(9)				dB
Level Separation Mismatch Ratio	T_RLM	See(10) (11)(12)	0.95			%
Steady-State Voltage	T_Vf		0.4		0.6	V
Linear Fit Pulse Peak	T_Pk		0.80 x T_Vf			V
Signal-to-Noise-and-Distortion-Ratio	T_SNDR		31			dB

2.4.2. Transmitter Return Loss

The following figure details the minimum permitted MR transmitter differential return loss (RL) for 29 Gbaud/s. Notice that RLmin is -6 dB at 14.5 GHz. Using the equation for differential return loss limit below, with f = 14.5, fb = 29, the result is RLmin = 6.09 dB. This is roughly the same as the RL for an NRZ system, which means that the transmitter operates roughly the same with existing legacy backplanes.

(6) Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.

(7) Measured as described in Section 17.3.1.2 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04.

(8) See Equation 17-4 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04

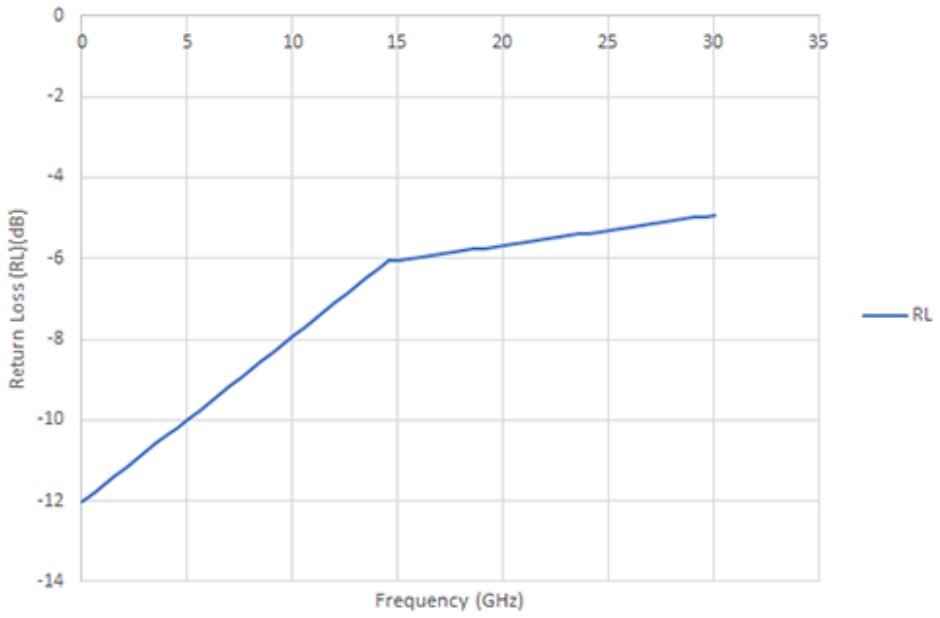
(9) See Equation 17-5 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04

(10) Signals are specified as measured through a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth.

(11) Measured as described in Section 17.3.1.2 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04.

(12) Measured as described in Section 17.3.1.6 of the *CEI-56G-MR-PAM4 Medium Reach Interface*, OIF2014.245.04.

Figure 13. Transmitter Differential Return Loss Limit for 29 Gbaud/s (58 Gbps)



Equation 4. Differential Return Loss Limit

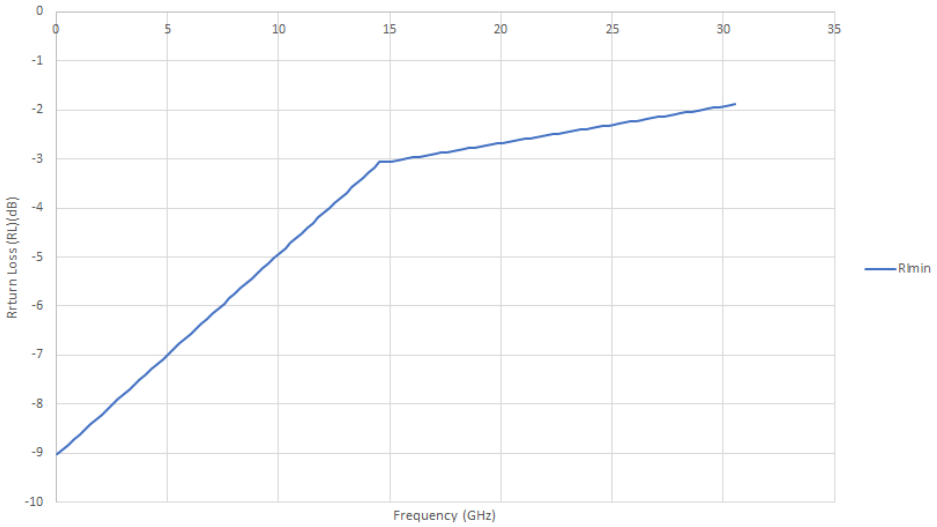
$$RL_d(f) \geq RL\min(f) = \begin{cases} 12.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5 f_b) \\ (-1)\,(\quad) & \\ 7.175 - 0.075\left(\frac{f \times 29}{f_b}\right) & (0.5 f_b \leq f \leq f_b) \end{cases} (dB)$$

From the figure, RLmin is -3 dB at 14.5 GHz. Using the equation for common mode return loss limit below, with f = 14.5, fb = 29, results in RLmin = 3.09 dB.

Figure 14. Transmitter Common Mode Return Loss Limit for 29 Gbaud/s (58 Gbps)

RLmin is -3 dB at 14.5 GHz.

RLmin = 3.09 dB using Equation 5 on page 17 where f = 14.5 and fb = 29.



Equation 5. Common Mode Return Loss Limit

$$RL_C(f) \geq RL\min(f) =$$
$$9.05 - 0.4112\left(\frac{f \times 29}{f_b}\right) \quad (0.05 \leq f \leq 0.5 f_b)$$
$$(-1)\,(\qquad\qquad\qquad\qquad)\,(dB)$$
$$4.175 - 0.075\left(\frac{f \times 29}{f_b}\right) \quad (0.5 f_b < f \leq f_b)$$

2.4.3. Transmitter Linearity (R_{LM})

The Level Separation Mismatch Ratio, commonly referred to as R_{LM}, is a measurement that is not required in normative or informative VSR tests, but is required by most other variants.

R_{LM} is conceptually similar to eye linearity but measured differently. An ideal PAM4 eye has R_{LM} equal to 1, but it does not scale in the same way as eye linearity. The four voltage levels of PAM4 are V_0, V_1, V_2 and V_3 respectively. The mid-range level V_{mid} is defined in Equation 6 on page 17. The mean signal levels are normalized and offset adjusted so that V_{min} corresponds to 0, V_0 to -1, V_1 to -ES1, V_2 to ES2 and V_3 to 1.

The mean signal levels described above are measured from a waveform captured while the transmitter is transmitting the QPRBS13-CEI test pattern. The waveform consists of M samples per unit interval and is aligned such that the first M samples of the waveform correspond to the first PAM4 symbol of the test pattern, the second M samples to the second PAM4 symbol, and so on. This allows each sample of the waveform to be associated with a specific PAM4 symbol in the test pattern.

Equation 6. V_{min} Calculation

$$V_{\min} = \frac{V_0 + V_3}{2}$$

Equation 7. ES1 Calculation

$$ES1 = \frac{V_1 - V_{min}}{V_0 - V_{min}}$$

Equation 8. ES2 Calculation

$$ES2 = \frac{V_2 - V_{min}}{V_3 - V_{min}}$$

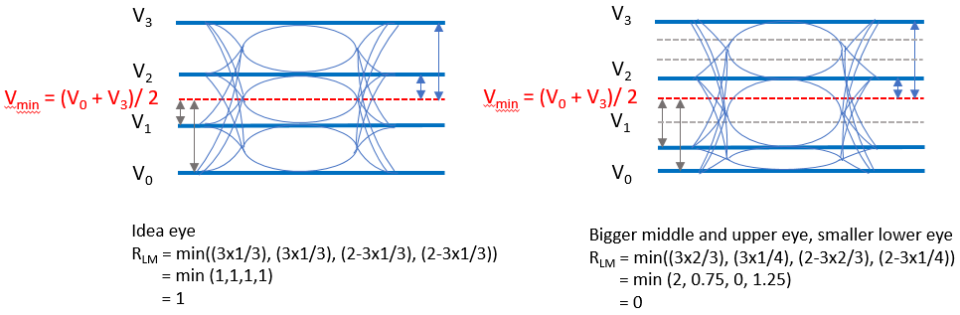
Equation 9. R_{LM} Calculation

$$R_{LM} = \min((3 \times ES1), (3 \times ES2), (2 - 3 \times ES1), (2 - 3 \times ES2))$$

For an ideal eye, three eye heights are the same. The distance of V_1 to V_{min} is one third of the distance of V_0 to V_{min}. In the same manner, the distance of V_2 to V_{min} is one third of the distance of V_3 to V_{min}. Using Equation 9 on page 18, R_{LM} equals to 1. The second figure shows an eye that does not have very good eye linearity. V_1 moved lower to a point that the distance of V_1 to V_{min} is two thirds of V_0 to V_{min}. V_2 moved lower to a point that the distance of V_2 to V_{min} is one quarter of the distance of V_3 to V_{min}.

When using Equation 9 on page 18, the calculated R_{LM} is equal to 0. For the MR standard, the minimal acceptable linearity is 0.95, which roughly translates to a 5% error on the linearity of the eye. The closer R_{LM} is to 1, the better the eye linearity is.

Figure 15. R_{LM}



2.4.4. Signal-to-Noise-and-Distortion Ratio (SNDR)

SNDR uses linear fit pulse response (p(k)) and linear fit error (e(k)), which is the difference between the actual transmitter output signal and the ideal signal. SNDR is the variation between the ideal signal and the measured signal for a specified number of measurements. It is calculated using p(k) and e(k). As shown in the following equation, where p_{max} is the maximum value of p(k), $sigma_e$ is the standard deviation of e(k). $sigma_n$ is an average number of 4 measurements of RMS deviation of the PAM4 voltage levels.

Equation 10. Signal-to-Noise-and-Distortion Ratio

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

SNDR must be at a minimum 31 dB according to the OIF-56G-MR transmitter specification.

SNDR is measured at the transmitter output with transmitters on all lanes enabled and transmitting the QPRBS13-CEI pattern, with at least 14 symbol periods of delay between each lane and with identical transmit equalizer settings.

2.5. PAM4 Jitter Methodology

Many NRZ signal standards require extrapolation of Total Jitter (Tj) to BERs of 10^{-12}. This required fitting values to a (dual-dirac) model. Total Jitter (Tj) includes Random Jitter (Rj) and Deterministic Jitter (Dj), which are determined by that extrapolation method. PAM4 technologies require only a BER of 10^{-6} at the physical layer. Since oscilloscopes can easily acquire 10^6 bits in a single acquisition, Rj/Dj extrapolation is not required, and a new methodology is used for PAM4 signaling.

Table 6. Transmitter Output Jitter Specifications

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Uncorrelated Bounded High Probability Jitter	T_UBHPJ	See (13)			0.05	UIpp
Uncorrelated Unbounded Gaussian Jitter	T_UUGJ				0.01	UIrms
Even-Odd Jitter	T_EOJ				0.019	UIpp

Uncorrelated Unbounded Gaussian Jitter (UUGJ) is conceptually similar to Rj. Uncorrelated Bounded High Probability Jitter (UBHPJ) is conceptually similar to Dj. Even-Odd Jitter (EOJ) is a new method for PAM4. EOJ is measured from a specific pattern PRBS13Q defined in the OIF-56G standard.

The methodology used to measure UUGJ, UBHPJ and EOJ is defined in section 17.3.1.7.1 of the OIF-CEI-56G-MR standard.

2.6. TX Pre-Emphasis Method

When signals travel through a lossy backplane, signal transitions can expand to adjacent intervals. This effect is known as Inter-Symbol Interference (ISI). The purpose of TX pre-emphasis is to apply delay and inversion to the signal and add it back to the original signal with the proper weight, thereby compensating for ISI from the nearby data symbol.

The transmitter equalization requirements for each CEI standard are defined in their respective COM specifications. Refer to *CEI-56G-MR-PAM4 Interface Details* for more information about transmitter equalization requirements. These are the minimum expected pre-emphasis requirements. For an MR channel, there are only three taps:

- Main cursor
- Pre-cursor
- Post-cursor

(13) Measured as described in Section 17.3.1.7

Table 7. MR COM Specifications

Parameter	Symbol	Value	Units
Signaling rate	f_b	18 - 29	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Transmission line characteristic impedance Single-ended package capacitance at package-to-board interface	 C_d z_p z_p Z_C C_p	 160 12 30 85 110	 fF mm mm Ω fF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	0.75 x f_b	
Transmitter equalizer, minimum cursor	c(0)	0.60	-
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	c(-1)	 -0.15 0 0.05	 - - -
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	c(1)	 -0.25 0 0.05	 - - -
Continuous time filter, DC gain Minimum value Maximum value Step size	gDC	 -15 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	gDC2	 -5 0 1	 dB dB dB
Continuous time filter, zero frequencies	f_z f_{z2}	f_b/2.5 f_b/40	GHz GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2} f_{p3}	f_b/2.5 f_b/40 f_b	GHz GHz

Related Information

CEI-56G-MR-PAM4 Interface Details on page 22

3. CEI-56G-MR-PAM4 Interface Details

This chapter details the electrical interface between nominal baud rates of 18 Gsym/s (36 Gbps) and 29 Gsym/s (58 Gbps) using PAM4 coding.

The signal trace or channel between a transmitter and a receiver must meet the Channel Operating Margin (COM) specification, a method and a threshold quantity used for channel compliance. The COM specification table is normative (mandatory). The insertion loss (IL) or return loss (RL) formulas or graphs are only informative (recommended).

3.1. COM Introduction

The Figure of Merit (FOM) of one specific channel, which is regulated by the COM specification, is fixed no matter what transceiver is used. This is because the FOM parameter describes the quality of a channel. FOM is calculated using S-parameters: insertion loss, insertion loss deviation, return loss, integrated crosstalk noise and a number of coefficients that are based on the specific standard. The MR coefficients are described in Table 8 on page 22.

Table 8. FOM for Two Backplanes

Test 1 uses a short package, and Test 2 uses a long package. These are reference package traces. The FOM calculation for the backplanes measurements shown in Backplane Measurements on page 23 are reported for the 26.25-inch channels. This table shows that the Nelco channel would fail test 2 for a basic 26.25-inch NRZ channel. However, the same channel would pass PAM4 due to the mandatory FEC needed when transmitting a PAM4 signal.

Backplane Measurement	NRZ		NRZ w/ FEC		PAM4	
	Test 1	Test 2	Test 1	Test 2	Test 1	Test 2
Megtron 20"	4.72	4.46	8.44	8.21	6.68	6.86
Megtron 26.25"	4.23	3.66	7.94	7.41	6.67	6.70
Megtron 32.5"	3.31	**2.61 (F)**	7.06	6.39	6.46	6.39
Megtron 38.75"	**1.84 (F)**	**0.98 (F)**	5.68	4.86	5.99	5.80
Nelco 20"	4.53	4.02	8.25	7.80	7.34	7.17
Nelco 26.25"	3.02	**2.33 (F)**	6.81	6.16	6.83	6.58
Nelco 32.5"	**1.25 (F)**	**0.41 (F)**	5.13	4.33	6.19	5.87
Nelco 38.75"	**-1.29 (F)**	**-2.44 (F)**	**2.66 (F)**	**1.61 (F)**	5.22	4.67

Note: Failing test results are highlighted in bold font, followed by an (F).

3.1.1. Backplane Measurements

The following figures are the measurement results for two backplanes, one using Megtron 6 and one using Nelco 26.25-inch backplanes. The measurements that calculate FOM include:

- Insertion loss (IL)
- Insertion loss deviation
- Return loss (RL)

Figure 16. Megtron 6 Insertion Loss

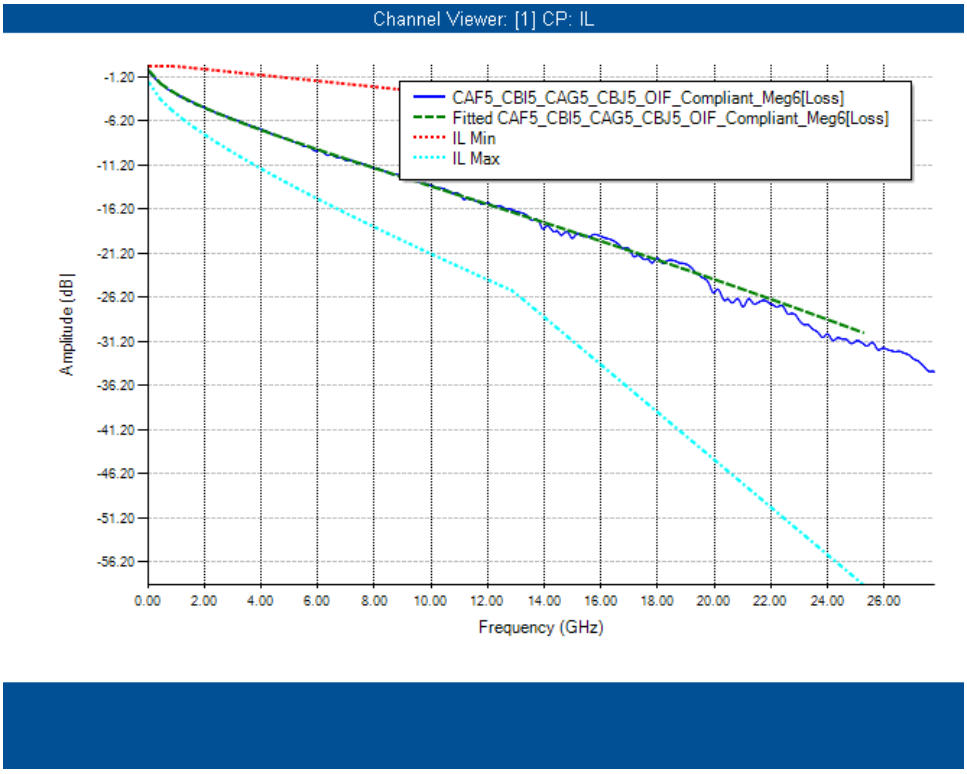


Figure 17. Megtron 6 Insertion Loss Deviation

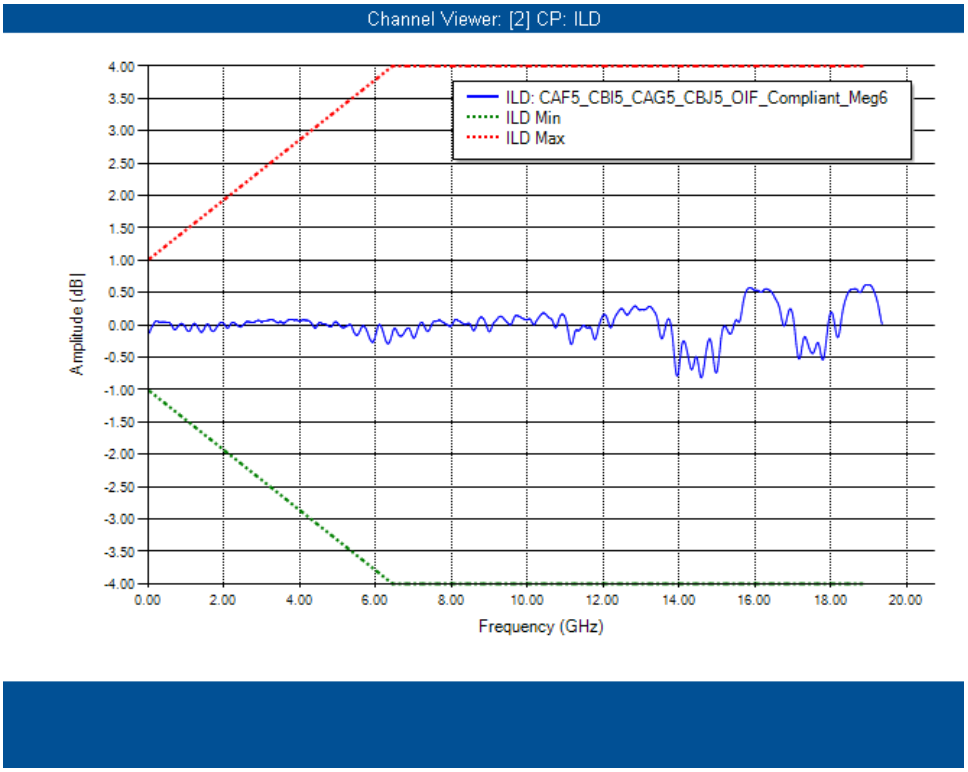


Figure 18. Megtron 6 Return Loss

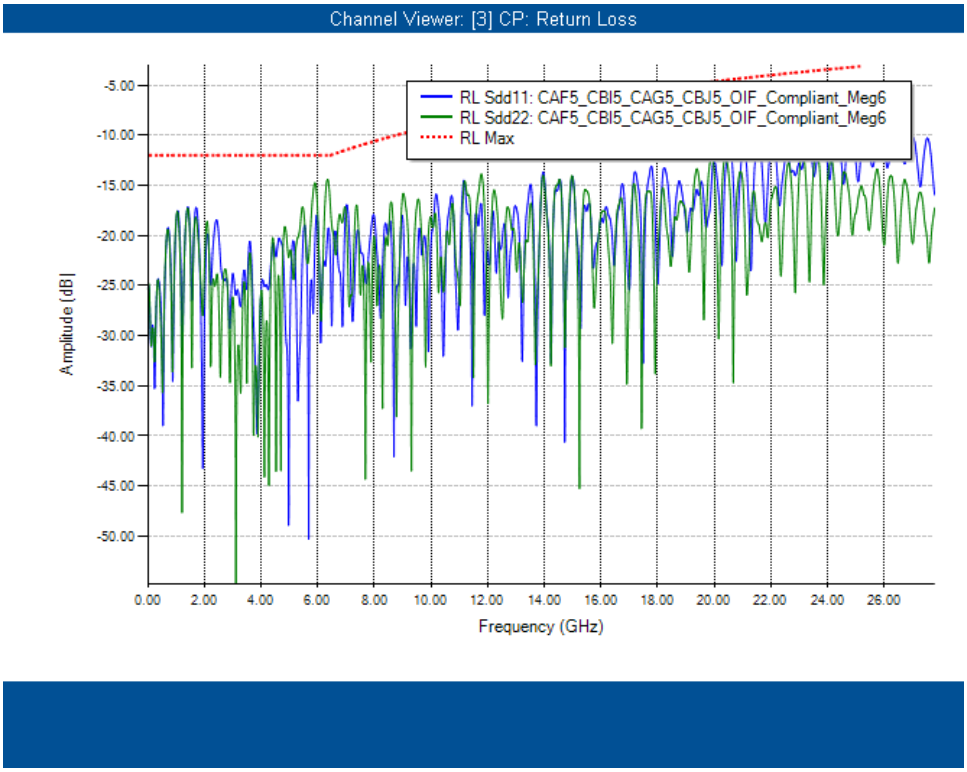


Figure 19. Nelco Insertion Loss

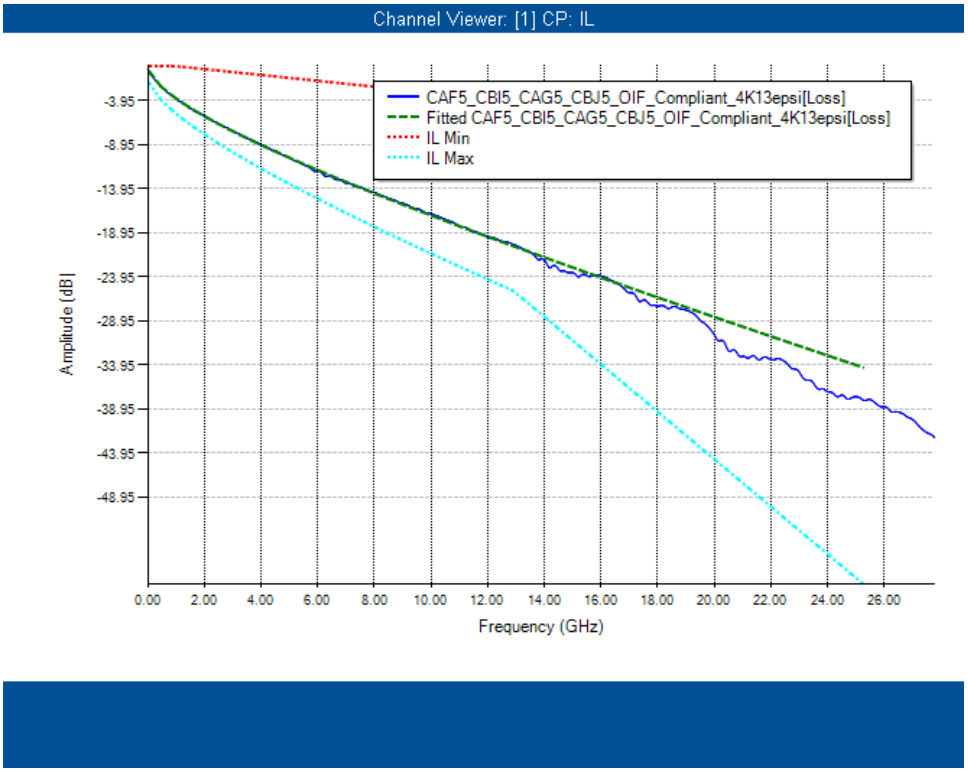


Figure 20. Nelco Insertion Loss Deviation

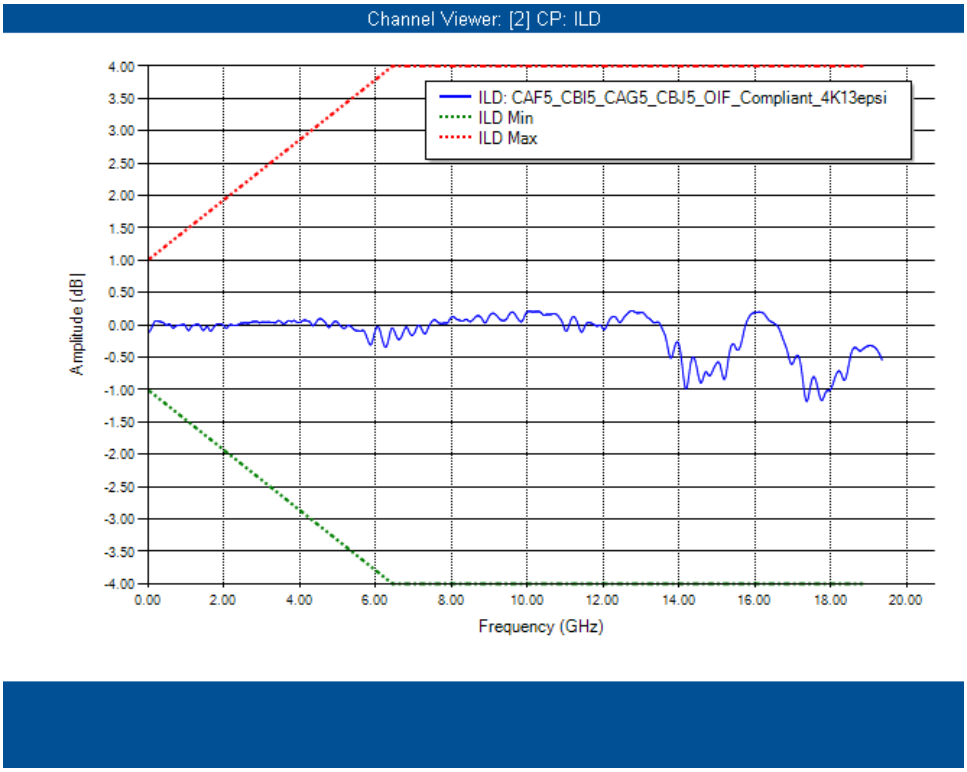
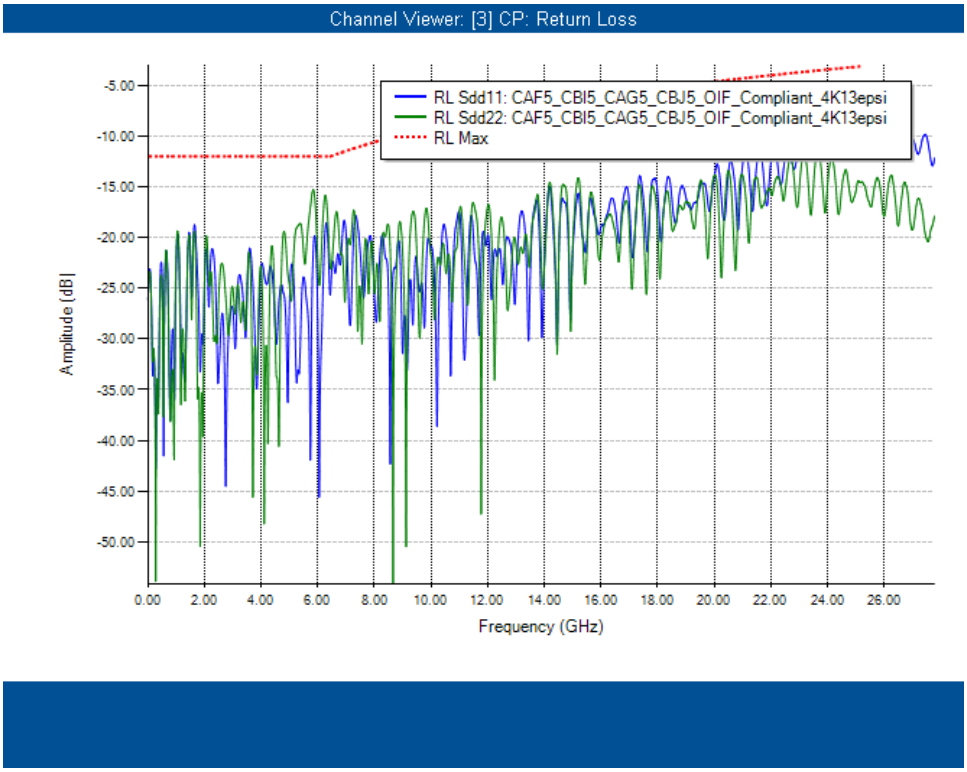


Figure 21. Nelco Return Loss



The bigger the FOM value, the better the quality of a channel. To pass the backplane FOM with the NRZ, NRZ with FEC, and PAM4 schemes, the channel's quality should be at least 3 dB.

3.2. Normative Channel Specification COM

These COM specifications shows the minimal mandatory requirements for an MR OIF-CEI channel.

Table 9. COM Specifications for MR

Parameter	Symbol	Value	Units
Signaling rate	f_b	18 - 29 (14)	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1	C_d z_p z_p Z_C C_p	160 12 30 85 110	fF mm mm Ω fF

continued...

(14) This signaling rate range equates to 36 Gbps to 58 Gbps.

Parameter	Symbol	Value	Units
Transmission line length, Test 2 Transmission line characteristic impedance Single-ended package capacitance at package-to-board interface			
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	0.75 x f_b	
Transmitter equalizer, minimum cursor	c(0)	0.60	-
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	c(-1)	 -0.15 0 0.05	 - - -
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	c(1)	 -0.25 0 0.05	 - - -
Continuous time filter, DC gain Minimum value Maximum value Step size	gDC	 -15 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	gDC2	 -5 0 1	 dB dB dB
Continuous time filter, zero frequencies	f_z f_{z2}	f_b/2.5 f_b/40	GHz GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2} f_{p3}	f_b/2.5 f_b/40 f_b	GHz GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.43 0.43 0.63	 V V V
Number of signal levels	L	4	-
Level separation mismatch ratio	R_{LM}	0.95	-
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB

continued...

Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	-
Decision feedback equalizer (DFE) length	N_b	10	UI
Normalized DFE coefficient magnitude limit for n = 2 to N_b	$b_{max}(1)$ $b_{max}(2\text{-}N_b)$	0.5 0.2	-
Random jitter, RMS	RJ	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	0	2.6×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	-
Channel operating margin, min	COM	3	dB

A transmitter or receiver must ensure that it meets the values in that table at minimum to be able to claim compliance.

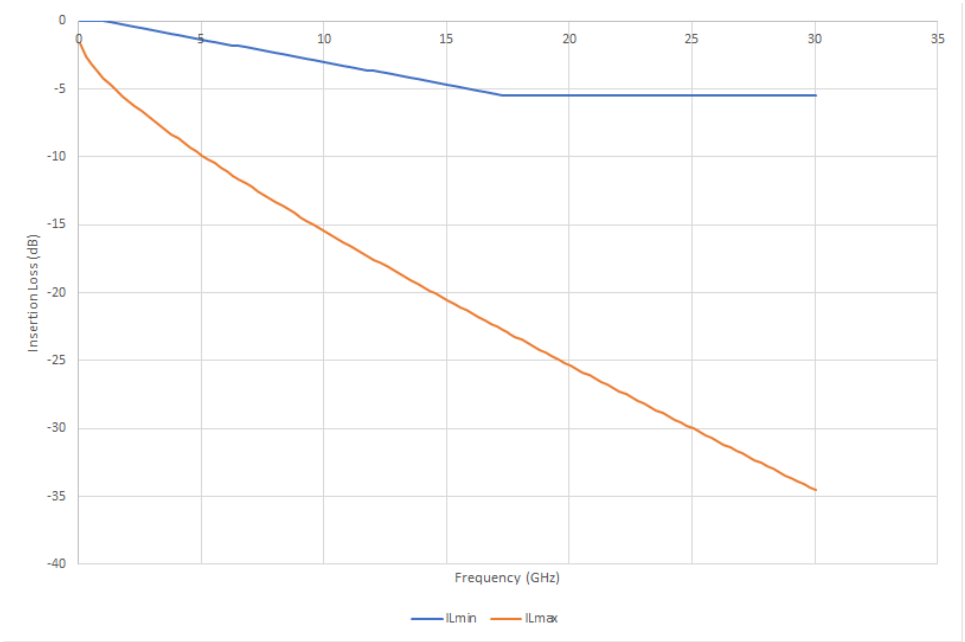
Each standard has a specific table.

3.3. Informative Channel Insertion Loss

For a channel to be considered MR, it must fit within the minimum or maximum envelope.

Figure 22. Channel Insertion Loss Limit for 29 Gsym/s (58 Gbps/s)

An MR channel would range from approximately ILmin -4.8 dB to ILmax -20 dB at 14.5 GHz. Use Equation 11 on page 31 and Equation 12 on page 31, with f = 14.5, fb = 29, ILmax = -20 dB, ILmin = -4.5 dB to calculate.



Channel insertion loss must be bounded by the following equations:

Equation 11. Maximum Insertion Loss

$$IL_{\max} = -\left[1.083 + 2.398\sqrt{\frac{f \times 29}{f_b}} + 0.676\frac{f \times 29}{f_b},\ f_{\min} \le f \le f_b\right]$$

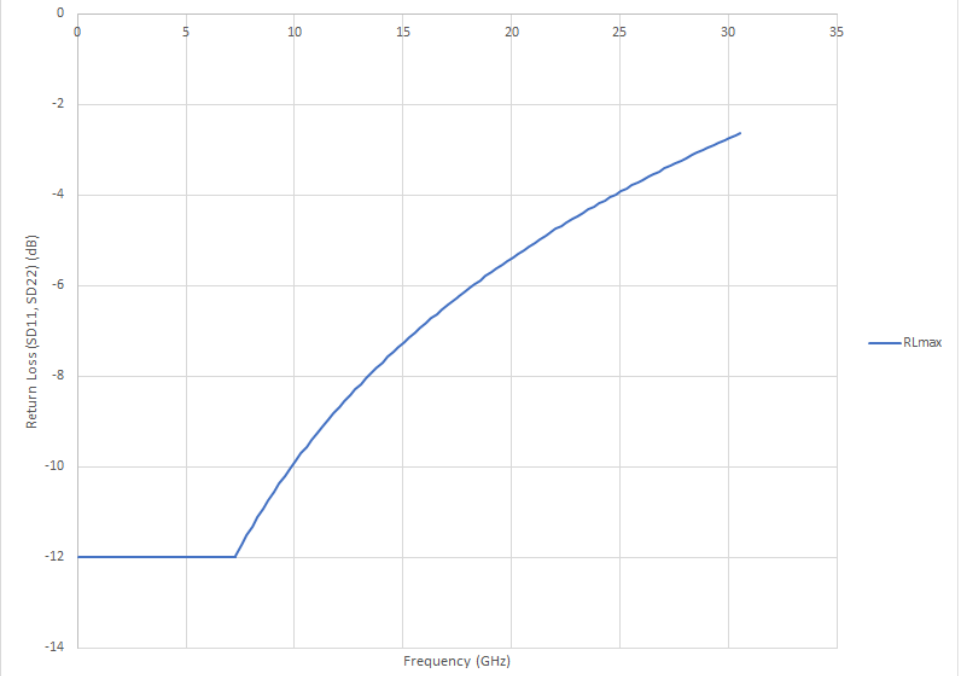
Equation 12. Minimum Insertion Loss

$$IL_{\min} = -\begin{cases} 0, & f_{\min} \le 1\,GHz \\ \frac{1}{3}(f-1), & 1\,GHz \le f \le 17.5\,GHz \\ 5.5, & 17.5 < f \le f_b \end{cases}$$

3.4. Informative Channel Return Loss

Figure 23. Channel Return Loss Limit for 29 Gsym/s (58 Gbps/s)

The minimum permitted return loss (RL) (abstract value) for the medium range (MR) channel. For a channel to be considered MR, it must exceed the minimum threshold. The following figure shows that RLmin is -7.5 dB. Using Equation 13 on page 31, with f = 14.5, fb = 29, the result is RLmax = -7.48 dB.



Channel return loss must be bounded by Equation 13 on page 31.

Equation 13. Channel Return Loss Limit

$$RLf_{\max} = -\begin{cases} 12, & f_{\min} \le f \frac{f_b}{4} \\ 12 - 15\log_{10}\left(\frac{4f}{f_b}\right), & \frac{f_b}{4} \le f \le f_b \end{cases}$$

4. CEI-56G-MR-PAM4 Receiver

This chapter explains the basic receiver architecture to successfully detect PAM4 signals and recover the data with different equalization techniques (when required).

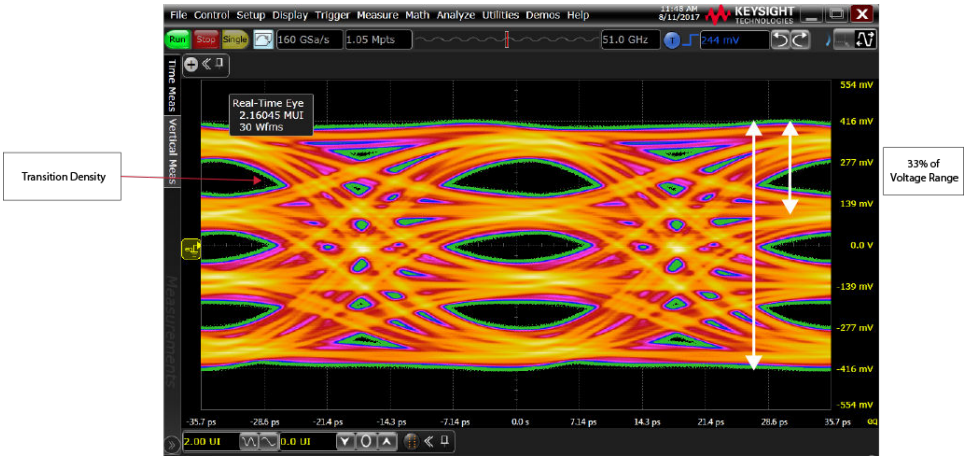
To understand the PAM4 receiver solutions, you should understand the various challenges associated with analyzing PAM4 signals.

4.1. Challenges in Analyzing PAM4 Signals

- **Sampling Point**: Finite rise times and different transition amplitudes create inherent ISI and make clock recovery more difficult. Consistent across all oscilloscope vendors, but quantization error plays a role when you take PAM4 measurements versus NRZ. Transition times of the PAM4 data signal can create significant horizontal eye closure due to higher transition density. The following figure shows the transition density.
- **Noise Tolerance**: Instead of having the full amplitude range, there is only 33% of the amplitude because the voltage range is divided into four levels (refer to the following figure). Lower PAM4 insertion loss compensates for the 9.5-dB loss in SNR.

  Because the eye height for PAM4 is 1/3 of the eye height for NRZ, **SNR loss = 20 * $\log_{10}(1/3)$ = ~9.5 dB**. When other non-linearity is included, it is approximately 11 dB.
- **Non-Linear Eyes**: System margin bottleneck lies with the **worst eye**. Non-linearity starts right at the TX output, and is composed of R_{LM} loss + SNDR loss + other losses like SNDR (ISI). For more details, refer to the *Eye Linearity* section.

Figure 24. Scope Capture of PAM4 Signal



Related Information

Eye Linearity on page 13

4.2. PAM4 Receiver Architecture

While the receiver architecture includes the basic modules required in a PAM4 serial link, it does not include architectural details of the Intel Stratix 10 PAM4 receiver solution.

4.2.1. Analog vs. Digital Receiver

Transition times of the PAM4 data signal can create significant horizontal eye closure due to the transition noise, which is dependent on the rise and fall times of the signal. Transition-qualified phase detectors are needed to look at analog levels for clock recovery.

Legacy NRZ analog receiver design can be leveraged. However, direct detection (comparators for four amplitude levels) requires a lot of power. For multilevel transmission, PAM4, digital receivers prove to be more flexible and provide powerful signal processing techniques. This can be expensive because of the added architectural complexities.

4.2.2. Slicer

Unlike NRZ, PAM4 symbols (two bits/symbol) are represented by different voltage levels. Three slicers with varying voltage thresholds are required to detect the different amplitude levels for PAM4.

4.2.3. Clock and Data Recovery (CDR)

Clock and data recovery is one of the challenging functions in modern high-speed serial data transmission. Multilevel transitions make the NRZ CDR unusable. The most famous CDR technique, for PAM4, is baud-rate CDR. Some of the examples are as follows:

1. Mueller-Mueller phase detector-based CDR

   K. Mueller and M. Muller, *Timing Recovery in Digital Synchronous Data Receivers*, IEEE Transactions on Communications, vol. COM-24, no. 5, pp. 516-531, May 1976.

2. Minimum mean square error phase detector-based CDR

   E. Lee and D. Messerschmitt, Digital Communication, 2nd ed. Kluwer Academic Publishers, Massachusetts, 1997.

4.3. Equalization Technique

Channel equalizations are needed to achieve the designated bit error rate targets for most link configurations.

Continuous-time linear equalizer (CTLE), feed-forward equalizer (FFE), and decision-feedback equalizer (DFE) are still the dominant receiver equalization schemes. Most of the NRZ equalization techniques are transferable. However, there are certain distinctions and details that need further attentions in PAM4 signaling links.

- **Multiple and floating decision threshold levels**: The decision thresholds need to be determined adaptively based on the link configuration. This is usually done by using a dedicated adaptation loop that performs Automatic Gain Control (AGC) on the incoming waveform or adjusts the thresholds based on the statistics of the received signal.
- **Reduced equalization solution space**: In the NRZ scheme, a receiver can usually over-equalize (within certain range) a waveform without dramatically decreasing the error-free data recovery margins. Over-equalizing a signal often sharpens the transition times, which may help reduce the noise-to-jitter transfer and, hence, the clock recovery performance. In PAM4, this flexibility is largely taken away because over-equalization will deteriorate the adjacent symbols. This implies that the equalization needs to be more precise with a reduced solution space. Furthermore, the step size of a receiver equalizer with discrete levels, such as CTLE AC gain levels and FFE/DFE tap coefficients, usually needs to be reduced to achieve the precision goal.
- **Receiver nonlinearity effects**: Nonlinearity in receivers may introduce non-uniform and asymmetric eye shapes. The equalizer will need to implement compensation schemes to achieve optimal performance.

The details on receiver equalization are out of the scope of this document. Intel Stratix 10 transceivers are auto-adaptive for both NRZ and PAM4 signal recovery.

4.4. CEI-56G-MR-PAM4 Receiver Details

This section details the receiver requirement as per CEI-56G- MR-PAM4 specifications.

A compliant receiver must autonomously operate at the specified bit error rate (BER) with the worst-case combination of a compliant transmitter and a compliant channel. The receiver shall accept the differential input signal amplitudes produced by a compliant transmitter connected with minimum attenuation as specified in Figure 22 on page 30.

4.4.1. Electrical Characteristics

Table 10. Receiver Electrical Input Specification for MR

Parameter	Symbol	Value	Unit
Baud Rate	R_Baud	18.0 - 29.0	Gsym/s
Differential Input Return Loss	R_SDD11	Equation 4 on page 16	dB
Differential to Common Mode Input Conversion2	R_SCD11	Equation 11 on page 31	dB
Interference Tolerance	See "Receiver Interference Tolerance Parameters" table		
Jitter Tolerance	See "Receiver Jitter Tolerance Parameters" table		

Table 11. Receiver Interference Tolerance Parameters

Parameter	Test Value 1 (15)		Test Value 2 (15)		Unit
	Min	Max	Min	Max	
Pre-FEC Bit Error Ratio (BER)	10^{-6}		10^{-6}		N/A
COM including effects of broadband noise	3		3		dB
Insertion loss at Nyquist	10		10		dB
RSS_DFE4	0.05		0.05		N/A

Related Information

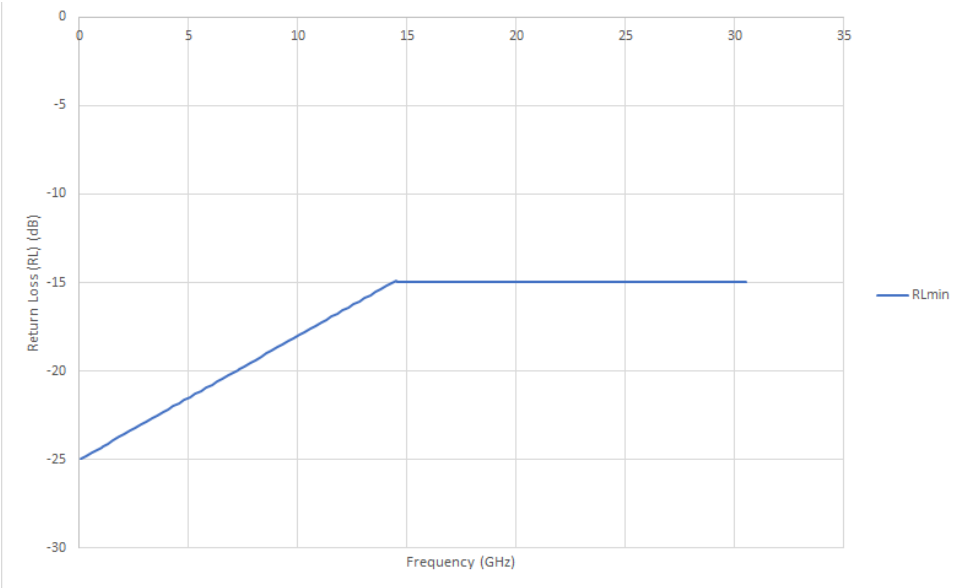
Normative Channel Specification COM on page 28

4.4.2. Receiver Input Return Loss

The differential input return loss, in dB, of the receiver must follow Equation 14 on page 36, with *f* being the frequency in GHz. The reference impedance for the differential return loss measurement is 100 Ω.

The differential to common-mode return loss, in dB, of the receiver must follow the equation below.

Figure 25. Receiver Differential to Common-mode Return Loss Limit for 29 Gsym/s



(15) Refer to *Normative Channel Specifcation COM* for details about what test values represent.

Equation 14. Differential to Common-Mode Return Loss

$$RL_{dc}(f) \geq RL\min(f) = \begin{cases} 25 - 0.6897\left(\frac{f \times 29}{f_b}\right) & (0.05 \leq f \leq 0.5 f_b) \\ 15 & (0.5 f_b < f \leq f_b) \end{cases} (dB)$$

4.4.3. Receiver Interference Tolerance

The receiver of each lane must meet the pre-FEC BER requirement with the channel matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 (refer to Table 9 on page 28).

The following considerations apply to the interference tolerance test:

- The test transmitter's measured SNDR should be used for SNRTX in the COM calculation
- The transmitter output levels are set such that RLM is equal to 0.95
- The test transmitter meets the specifications in the *CEI-56G-MR Transmitter* section.
- The test transmitter is constrained such that for any transmitter equalizer setting, the differential peak-to-peak voltage is less than 800 mV

Related Information

CEI-56G-MR Transmitter on page 11

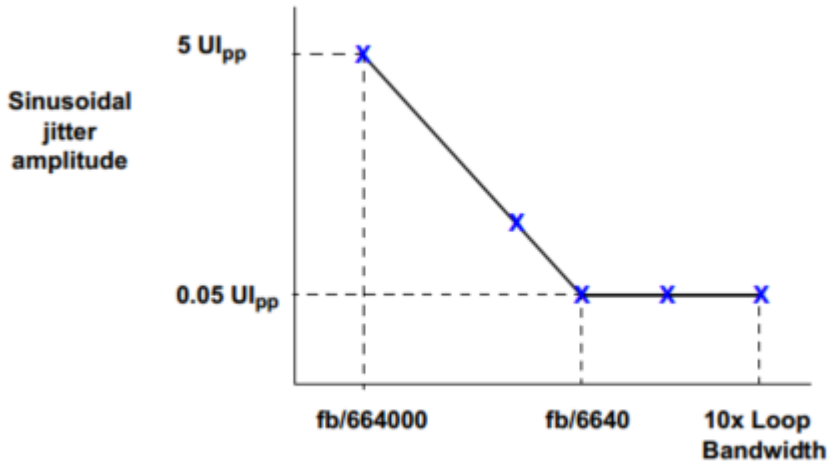
4.4.4. Receiver Jitter Tolerance

Receiver jitter tolerance must meet the conditions and parameters defined in the following table. This sinusoidal jitter is part of the jitter applied in the stressed input test. The receiver BER must be less than the maximum value for each pair of jitter frequency and peak-to-peak amplitude value listed in the table and figure below.

Table 12. Receiver Jitter Tolerance Parameters

Frequency Range	Sinusoidal Jitter, Peak-to-Peak (UI)
f < fb/664000	Not Specified
fb/664000 < f ≤ fb/6640	5 * fb / (664000 * f)
fb/6640 < f ≤ 10 times receiver loop bandwidth (fb/6640)	0.05

Figure 26. Receiver Jitter Tolerance Mask



5. PAM4 Link Case Study

This section shows the result from a case study on the following two links:

1. OIF_Stressed: Out of spec of CEI-OIF 56G MR spec
2. OIF_Compliant: Within spec of CEI-OIF 56G MR spec

Table 13. Channel Characteristics @ 14 GHz

Electrical Characteristics	CEI-56G-MR-PAM4 Spec (dB)	OIF_Stressed (dB)	OIF_Compliant (dB)
Insertion Loss	< 20.0	22.78	18.79
Return Loss	> 7.5	~14.5	~13.5
Channel Operating Margin (COM)	> 3.0	~3	~3.7

The link simulations were performed with the help of Intel's Advanced Link Analyzer. The transmitter and the receiver are both Intel Stratix 10 E-Tile IBIS-AMI models. The package models are added on top because they are not part of the device model. Hence, you observe separate TX and RX package models in the following figures for link simulation results.

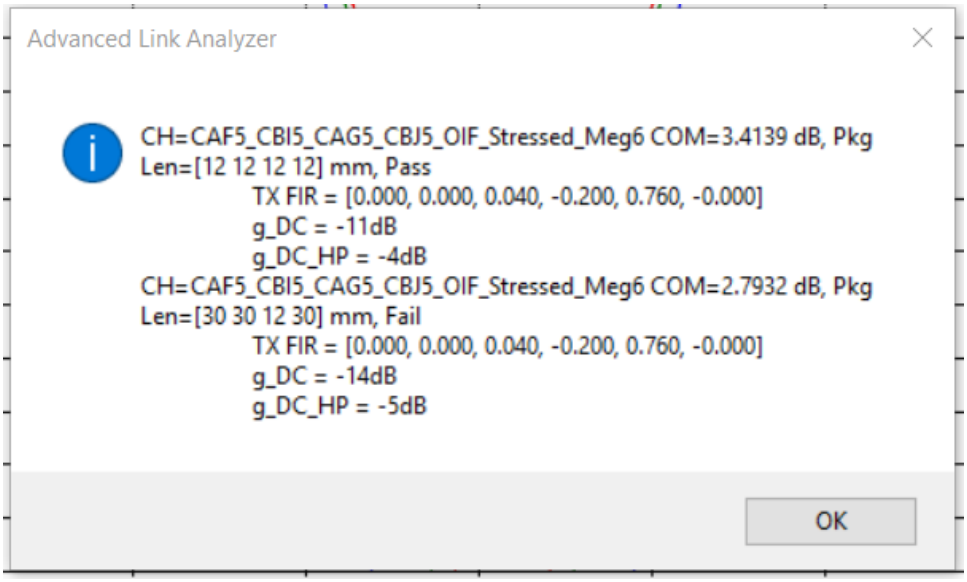
5.1. OIF_Stressed

COM Analysis was run on the channel under test using the Channel Viewer of Intel's Advanced Link Analyzer. The COM results were as follows:

- Short package length, COM (test 1) = 3.4139 dB, passing
- Long package length, COM (test 2) = 2.7932 dB, marginally failing

The link simulation was run on the typical TX and RX packages, ~22.6 mm. The channel is just passing with COM ~3 dB.

Figure 27. OIF_Stressed Channel Characteristics: COM Analysis Results for Test 1 and Test 2



5.1.1. Channel Characteristics

The following figure shows the characteristics of a channel used in the experiments. The channel's insertion loss (IL) is *~22.76 dB* at *14.0 GHz* and*~38 dB* at *25 GHz*. The insertion loss deviation (ILD) characteristics show that it has narrow *(<2.5 dB*) spread up to *~20 GHz*.

The characteristics indicate the channel should be fine for NRZ and PAM4 link operations up to *25GHz* , but it has difficulties supporting *50 Gbps* NRZ operation as both the ILD and IL deteriorate quickly after *25 GHz*.

Figure 28. OIF_ Stressed Channel Characteristics Insertion Loss (IL)

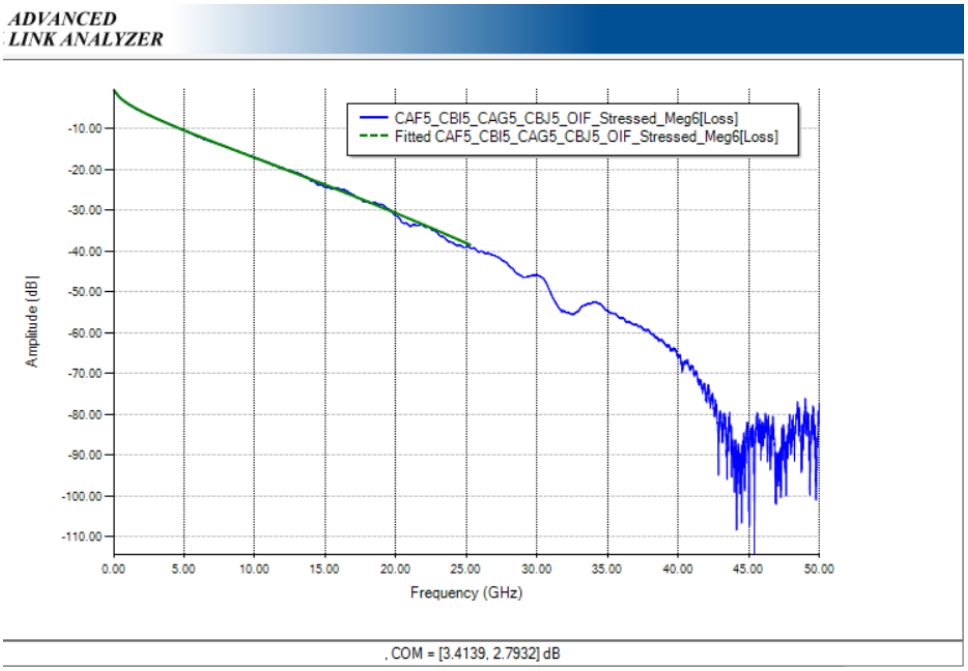


Figure 29. OIF_ Stressed Channel Characteristics Insertion Loss Deviation (ILD)

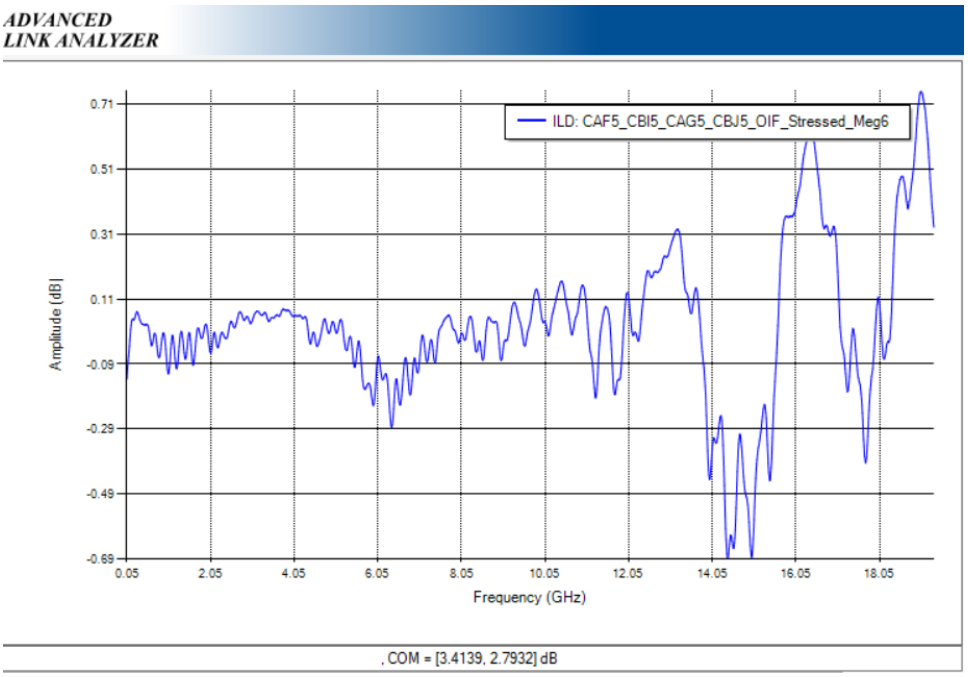
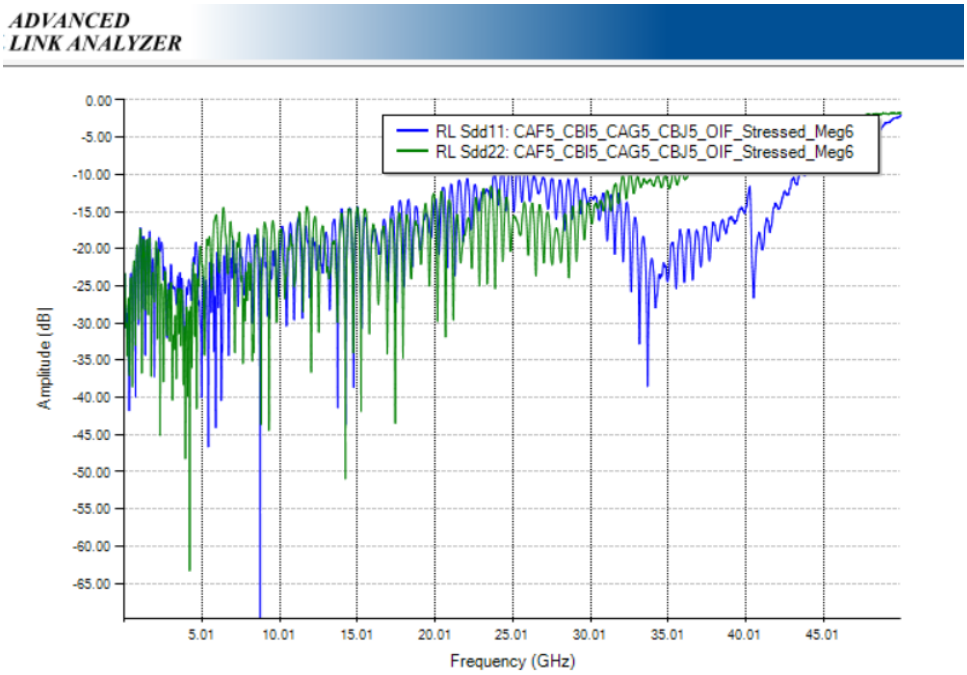


Figure 30. OIF_ Stressed Channel Characteristics Return Loss (RL)



5.1.2. OIF_Stressed PAM4 Link Simulation with the Advanced Link Analyzer

The schematic topology is as follows:

- **Transmitter (No Equalization)**: Intel Stratix 10 E-Tile, IBIS-AMI Model
- **TX Package**: Intel Stratix 10 TX Package
- **Transmitter Channel**: OIF Stressed Link
- **RX Package**: Intel Stratix 10 RX Package
- **Receiver (Adaptive)**: Intel Stratix 10 E-Tile, IBIS-AMI Model

Figure 31. OIF Stressed Link Simulation Results

(a) = TX eye diagram, (b) = Channel eye diagram, (c) = RX CDR eye diagram

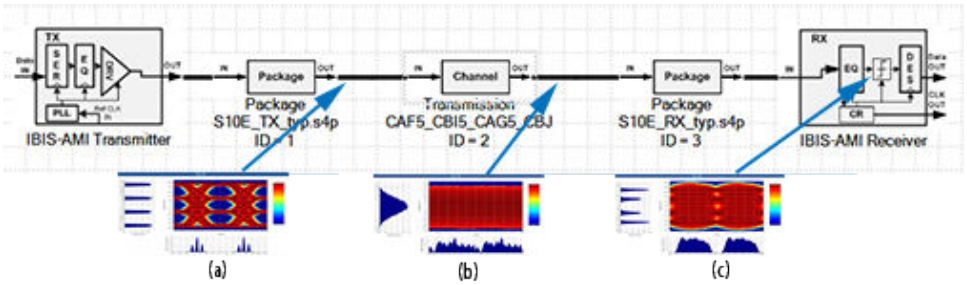


Figure 32. RX CDR BER Eye

A BER contour of 1E-6 (passing the CEI-OIF-56G MR spec).

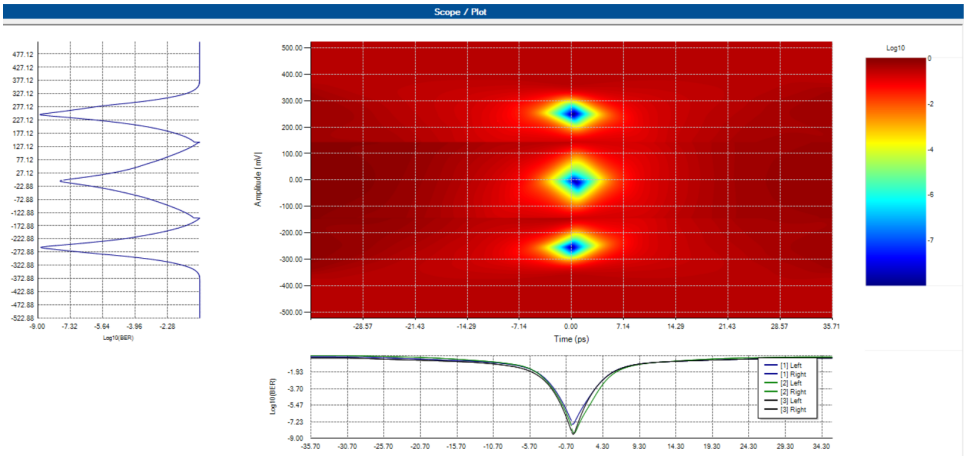
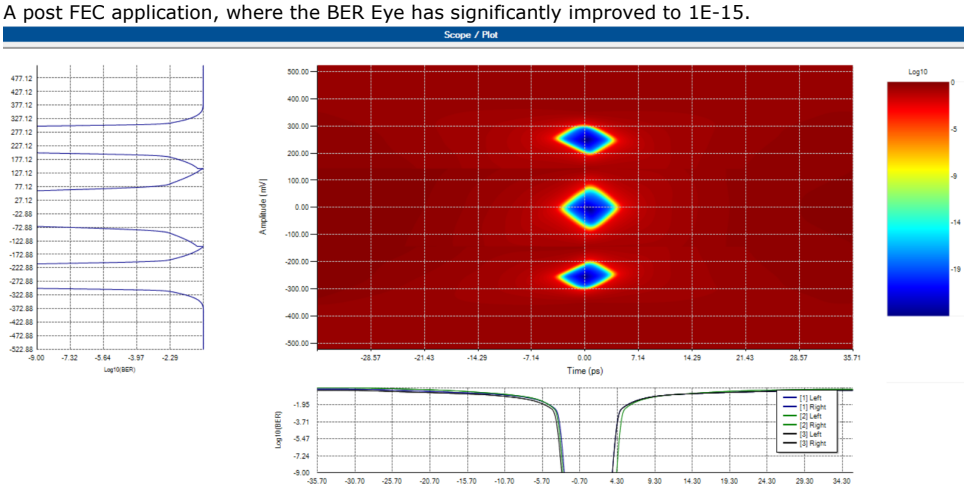


Figure 33. RX CDR FEC BER Eye

A post FEC application, where the BER Eye has significantly improved to 1E-15.



Advantage: Intel Advanced Link Analyzer can apply and provide RS FEC (544,514) projection to more accurately evaluate the channel performance. This is an unparalleled advantage compared to link simulation tools currently existing in the market.

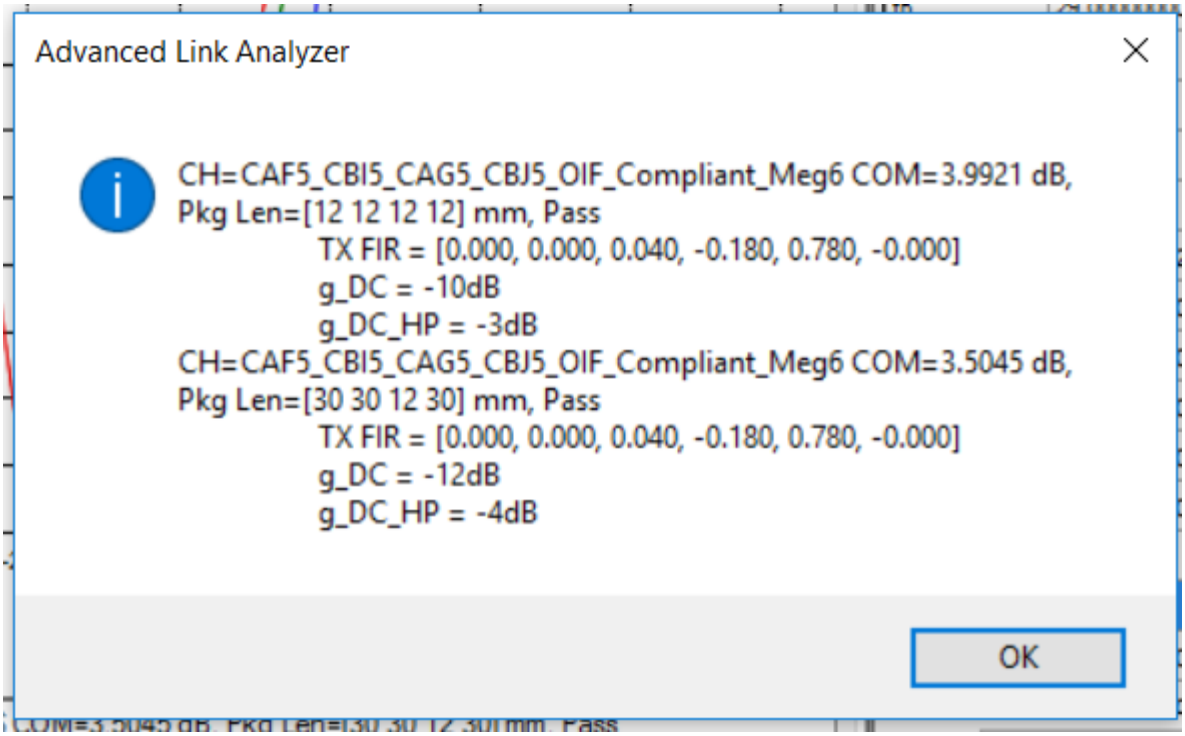
5.2. OIF_Compliant

COM analysis was run on the channel under test using the Channel Viewer of Intel's Advanced Link Analyzer. The COM results were as follows:

- Short package length, COM = 3.9921 dB, passing
- Long package length, COM = 3.5045 dB, passing

The link is clearly passing with a COM value of greater than 3 dB for both short-length and long-length packages.

Figure 34. OIF_ Stressed Channel Characteristics: COM Analysis Results for Long Reach and Short Reach



5.2.1. Channel Characteristics

The channel's insertion loss (IL) is *~18.79 dB* at *14.0 GHz* and *~31 dB* at *25 GHz*. The insertion loss deviation (ILD) characteristics show that it has narrow *(<1.8 dB*) spread up to *~20 GHz*.

Figure 35. OIF_Compliant Channel Characteristics: Insertion Loss (IL)

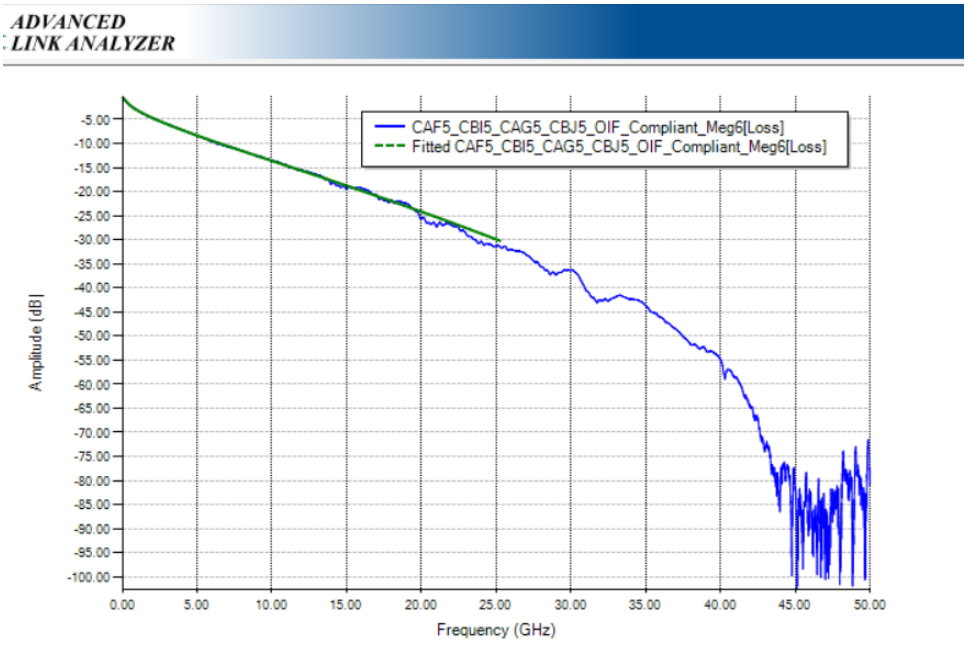


Figure 36. OIF_Compliant Channel Characteristics: Insertion Loss Deviation (ILD)

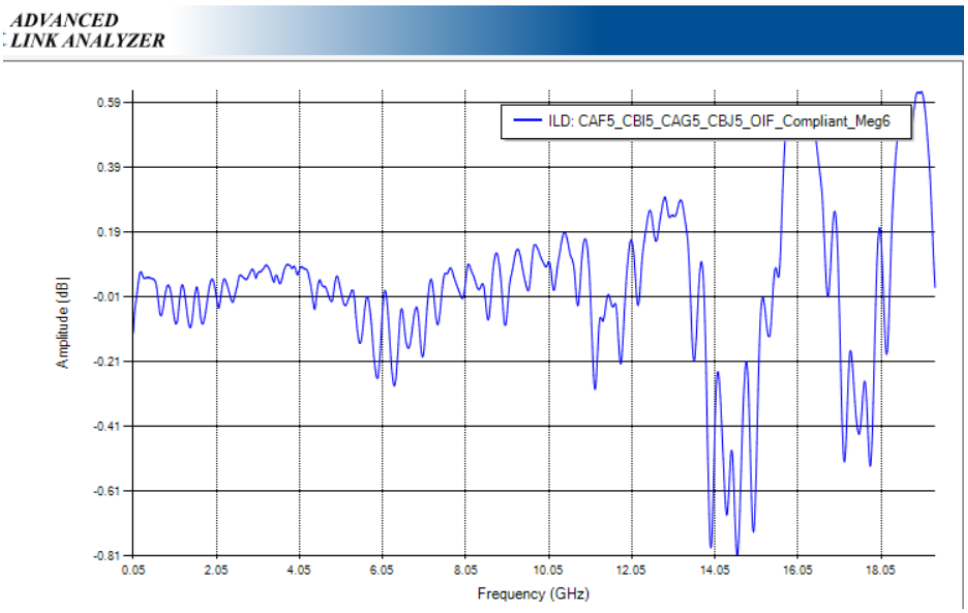
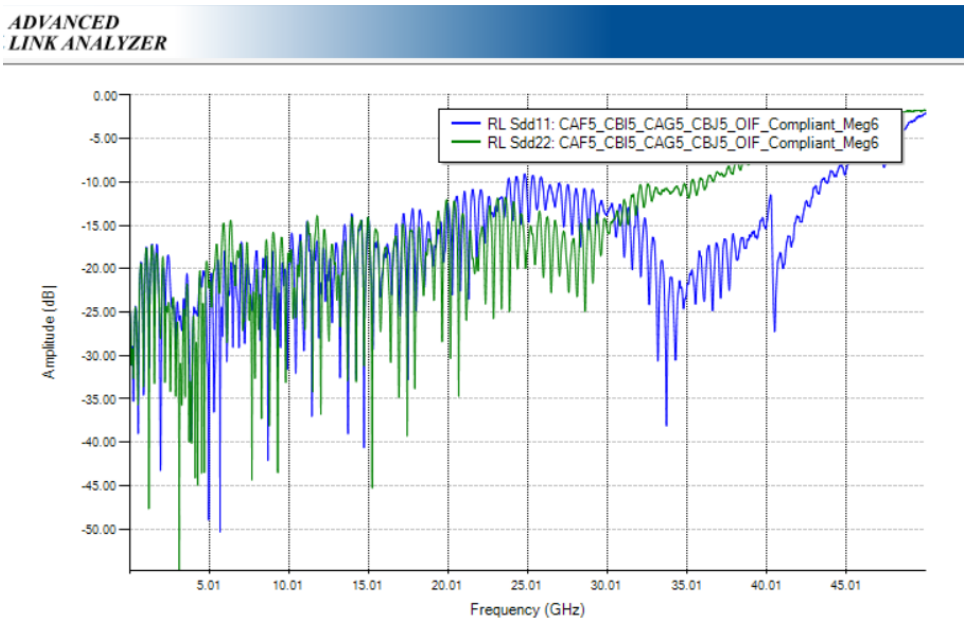


Figure 37. OIF_Compliant Channel Characteristics: Return Loss (RL)



5.2.2. OIF_Compliant PAM4 Link Simulation with the Advanced Link Analyzer

The schematic topology is as follows:

- **Transmitter (No Equalization)**: Intel Stratix 10 E-Tile, IBIS-AMI Model
- **TX Package**: Intel Stratix 10 TX Package
- **Transmitter Channel**: OIF Compliant Link
- **RX Package**: Intel Stratix 10 RX Package
- **Receiver (Adaptive)**: Intel Stratix 10 E-Tile, IBIS-AMI Model

Figure 38. OIF Compliant Link Simulation Results

(a) = TX eye diagram, (b) = Channel eye diagram, (c) = RX CDR eye diagram

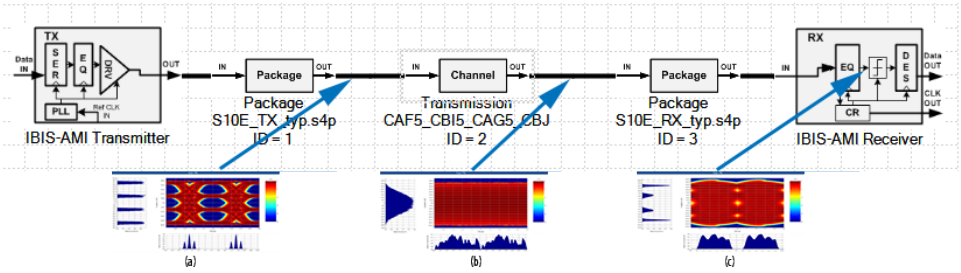


Figure 39. OIF Compliant Link Simulation Results: RX CDR BER Eye

A BER contour of 1E-7 (clearly passing the CEI-OIF-56G MR spec).

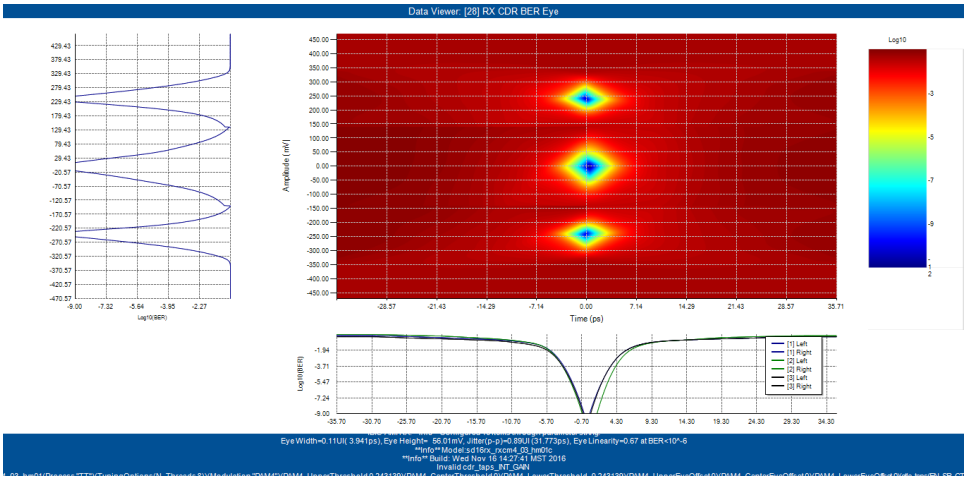
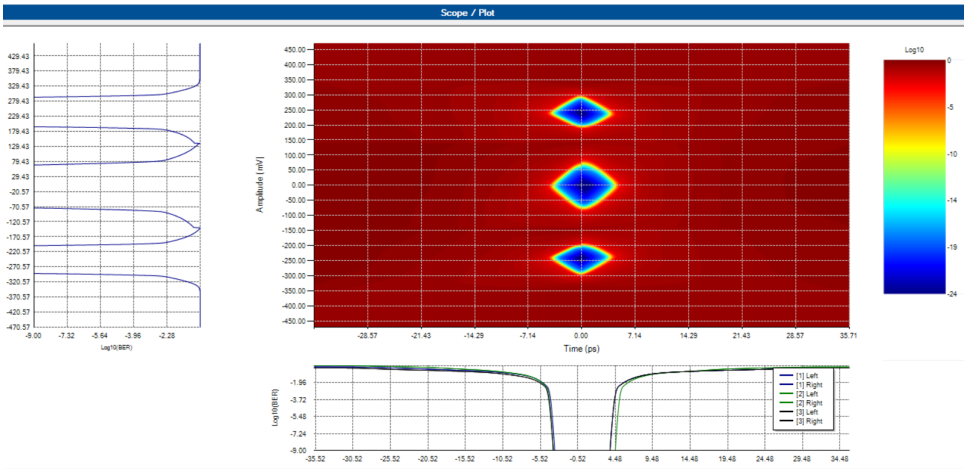


Figure 40. OIF Compliant Link Simulation Results: RX CDR FEC BER Eye

A post FEC application, where the BER eye has significantly improved to approximately 1E-18.



6. Medium Reach (MR) PAM4 System Design Study

This section provides a high-level discussion of the benefits of using PAM4 to design a MR OIF-CEI-56G-MR channel. It uses preliminary information available in the industry to illustrate the main benefits.

6.1. System Power

The following table shows how much power a PAM4 400 Gbps interface is expected to consume based on preliminary EPE calculations and module power.

Table 14. 4 x 100G System Power

There is a slight total power difference between NRZ and PAM-4 when PCS, FEC and PMA combined for total power (approximately 3.3 W).

Use Case	E-tile Power	Optics (QSFP-DD)	Normalized
4 x 100G w/ FEC + MAC (NRZ)	12.2 W	2 x 12 W	100%
4 x 100G w/ FEC + MAC (PAM4)	8.9 W	1 x 12 W	58%

However, by using PAM4, this interface only requires 1 QSFP-DD module rather than two (16 x 25 Gbps NRZ vs. 8 x 50 Gbps PAM4). This results in a total power saving of approximately 15 W.

In summary, this PAM4 interface saves 42% power when compared to the NRZ solution.

6.2. System Cost

Preliminary information indicates that the cost of a 400G module is approximately 2.4X that of a 100G module.

By extension, the cost of PAM4 optics is 40% less than the same legacy systems using four 100G modules. This does not factor in the additional board space, power and support components for that interface, which further adds to the cost.

6.3. Board Space

A QSFP-DD module has approximately the same width as a normal QSFP28 but twice the height.

Therefore, a 400-GBps interface using PAM4 and QSFP-DD requires less than ¼ of the same space required for QSFP28, assuming that the height of the modules is not problematic. You can place far more interfaces in the same footprint, assuming that power can be dissipated effectively.

6.4. Conclusion

PAM4 clearly offers power, footprint and cost advantages because of the reduced number of transceivers compared to an identical NRZ solution (1/2 the number of TX/RX).

However, because the power consumed is concentrated into a smaller footprint, designers of systems using PAM4 need to carefully plan out the power dissipation scheme. Refer to the *Intel Stratix 10 Device Design Guidelines* for information about how to plan your designs.

Related Information

Intel Stratix 10 Device Design Guidelines

7. Glossary and Acronyms

Table 15. Glossary of Terms

Terminology	Definition
CEI IA	A clause-based format supporting publication of new clauses over time
CEI-1.0	Includes CEI-6G-SR, CEI-6G-LR, CEI-11G-SR clauses
CEI-2.0	Added CEI-11G-LR clause
CEI-3.0	Added work from CEI-25G-LR, CEI-28G-SR
CEI-3.1	Includes CEI-28G-MR and CEI-28G-VSR
2.5D	A type of die-to-die integration via a silicon interposer having through-silicon vias (TSVs) connecting its top and bottom metal layers
3D	A three-dimensional (3D) integrated device in which two or more layers of active electronic components (e.g., integrated circuit dies) are integrated vertically into a single circuit where through-silicon vias (TSVs) are commonly used for die-to-die connection
Informative	Recommended
Normative	Mandatory

Table 16. List of Acronyms

Terminology	Definition
AGC	Automatic Gain Control
AUI	Attachment Unit Interface
CEI	Common Electrical Interface
COM	Channel Operating Margin
DMT	Discrete Multitone Modulation
ENRZ	Ensemble Non-Return to Zero
FEC	Forward Error Correction
FOM	Figure of Merit
IA	Implementation Agreements
LR	Long Reach
MCM	Multi-Chip Module
MR	Mid Reach
NRZ	Non-Return to Zero

continued...

Terminology	Definition
OIF	Optical Internetworking Forum
PAM-2	Pulse Amplitude Modulation 2 Levels
PAM-4	Pulse Amplitude Modulation 4 Levels
PCBA	Printed Circuit Board Assembly, an assembly of electrical components built on a rigid glass-reinforced epoxy-based board
PCBA	Printed Circuit Board Assembly
RS	Reed Solomon
SNDR	Signal-to-Noise and Distortion Ratio
SR	Short Reach
USR	Ultra Short Reach
VSR	Very Short Reach
XSR	Extra Short Reach

8. References

1. *Equalization and Clock Recovery for a 2.5-10 Gb/s PAM-2/PAM-4 Backplane Transceiver Cell*
2. *High Speed Baud-Rate Clock Recovery*
3. "Effects of Device Characteristics in Multi-Level Signaling Links"

9. Document Revision History for AN 835: PAM4 Signaling Fundamentals

Document Version	Changes
2019.03.12	Updated maximum transceiver data rates from 30 Gbps NRZ to 28.9 Gbps NRZ.
2018.01.31	Initial release.